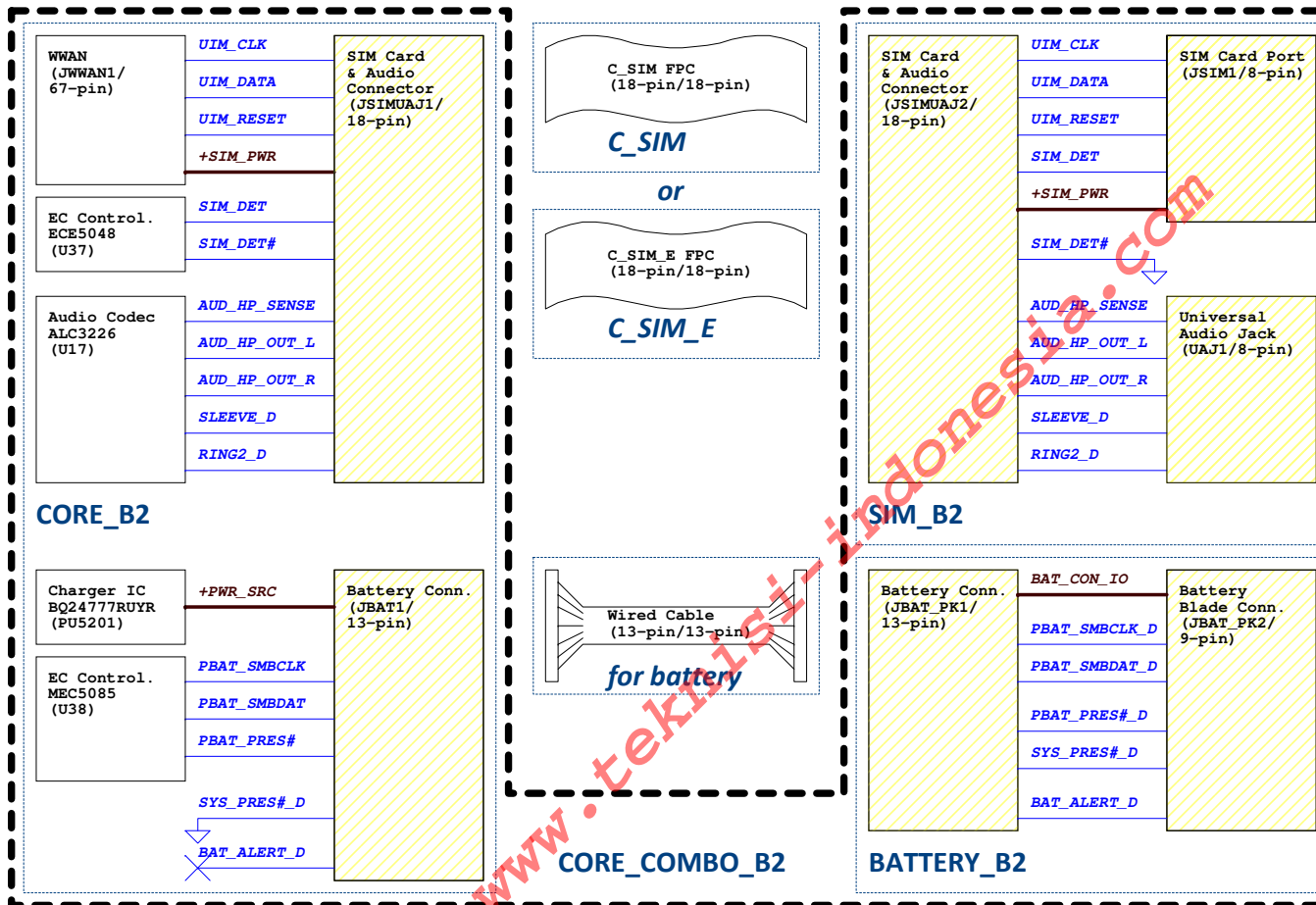


MCE2 A00 Reference Schematic

CORE_COMBO_B2 for Magellan / Columbus / Eriksson Gen2



Note: Net names here may not be consistent with real net names in the schematic.

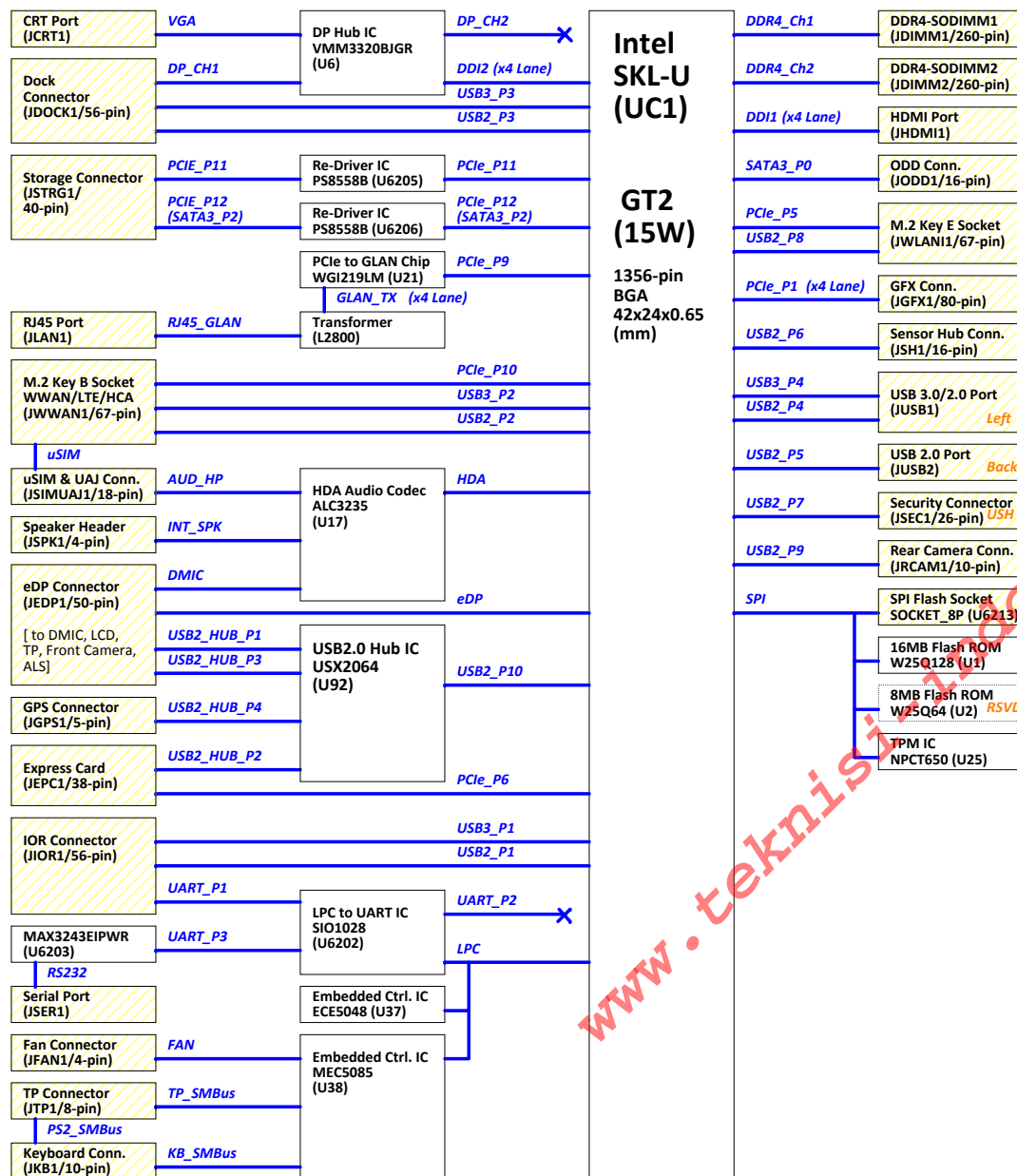
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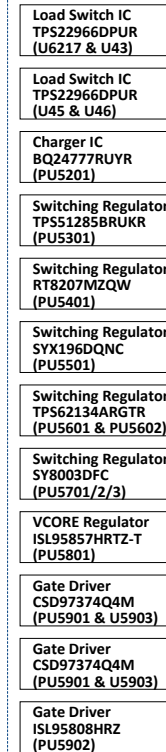
TITLE Cover Page	
DWG NO. CORE_COMBO_B2	REV. 2.0
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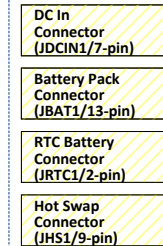
CORE_B2 System Block Diagram (A00)



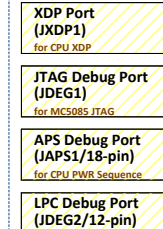
Power IC



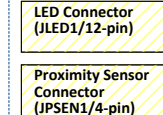
PWR Conn.



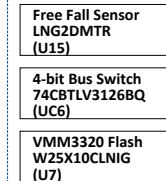
Debug Port



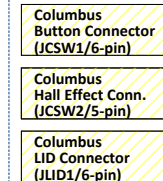
Misc. Conn.



Misc. IC



Col. Conn.



Note: Net names here may not be consistent with real net names in the schematic.

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DWG NO. CORE_B2	REV. 2.0		
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CORE_B2 Index and Configuraton (A00)

USB2.0 Port Map Configuration

SKL ULT	USB2.0	SCH Conf.	Destination	
	1	USB2_P1	IOR	(JIOR1)
	2	USB2_P2	WWAN	(JWWAN1)
	3	USB2_P3	DOCK	(JDOCK1)
	4	USB2_P4	USB3.0 Port	(JUSB1)
	5	USB2_P5	USB2.0 Port	(JUSB2)
	6	USB2_P6	Sensor Hub	(JSH1)
	7	USB2_P7	USH	(JSEC1)
	8	USB2_P8	Bluetooth	(JWLAN1)
	9	USB2_P9	Rear Cam	(JRCAM1)
	10	USB2_P10	USB Hub	(TS, FCam, EC/PC, GPS)

USH Configuration

USH		
0		BIO
1		NA

POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALW PLANE	M PLANE	SUS PLANE	RUN PLANE	CLK
State									
S0 (Full ON) with M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) with M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) with M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) with M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) with M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) with M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) with M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PCIe/USB3.0/SATA Port Map Configuration

USB3.0	SSIC	PCIE	SATA	SCH Conf.	Destination	
USB3.0 1				USB3_P1	IOR	(JIOR1)
USB3.0 2	SSIC 1			USB3_P2	WWAN	(JWWAN1)
USB3.0 3	SSIC 2			USB3_P3	DOCK	(JDOCK1)
USB3.0 4				USB3_P4	USB3.0 Port	(JUSB1)
USB3.0 5		PCIE 1		PCle_P1	GFX	(JGFX1)
USB3.0 6		PCIE 2				
		PCIE 3				
		PCIE 4				
		PCIE 5		PCle_P5	WLAN	(JWLAN1)
		PCIE 6		PCle_P6	Express/PC Card	(JEPC1)
		PCIE 7	SATA 0	SATA3_P0	ODD	(JODD1)
		PCIE 8	SATA 1	PCle_P8	N/A	(N/A)
		PCIE 9		PCle_P9	LOM	(U21)
		PCIE 10		PCle_P10	WWAN	(JWWAN1)
		PCIE 11	SATA 1*	PCle_P11&P12	SATA Express HDD	(JSTRG1)
		PCIE 12	SATA 2	SATA_P2		

PM TABLE

power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.0V_PRIM_CORE +1.0V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +VCC_CORE +VCC_GT	+3.3V_M	(M-OFF) +3.3V_M
State					
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/No AC	OFF	OFF	OFF	OFF	OFF

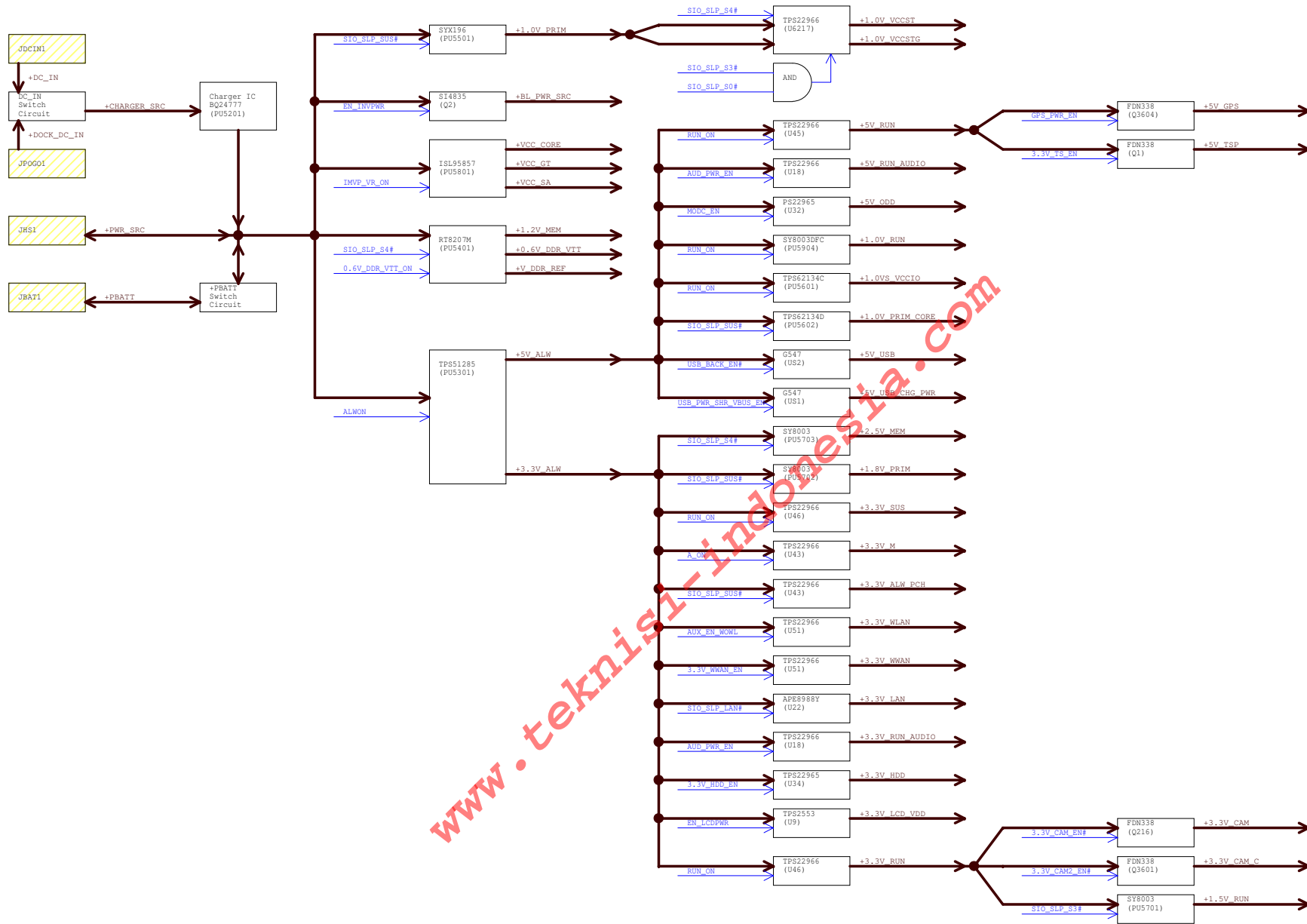
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TITLE Port Map
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CORE_B2 Power Rail (A00)



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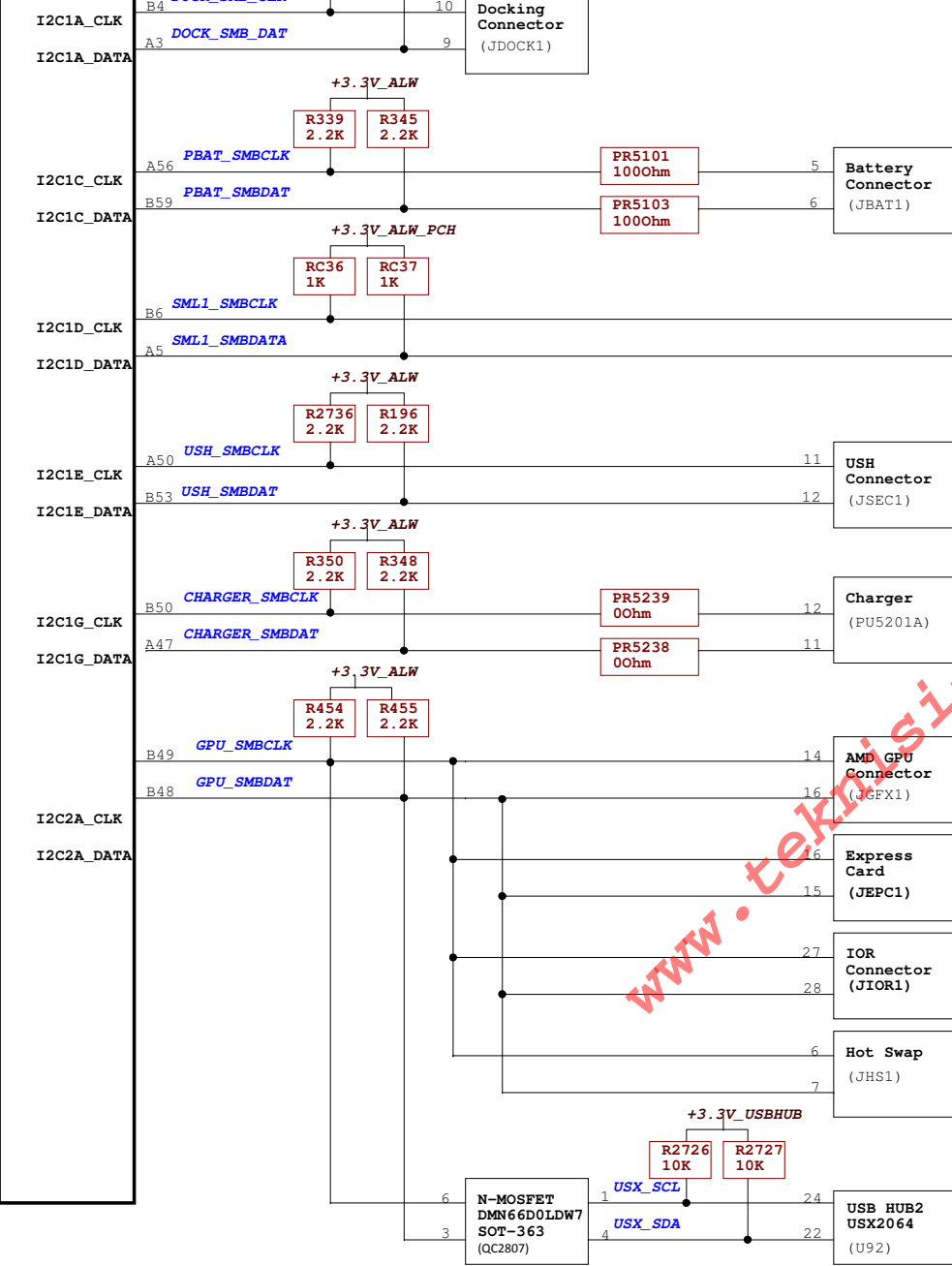
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TITLE Power Rail	
DWG NO. CORE_B2	REV. 2.0
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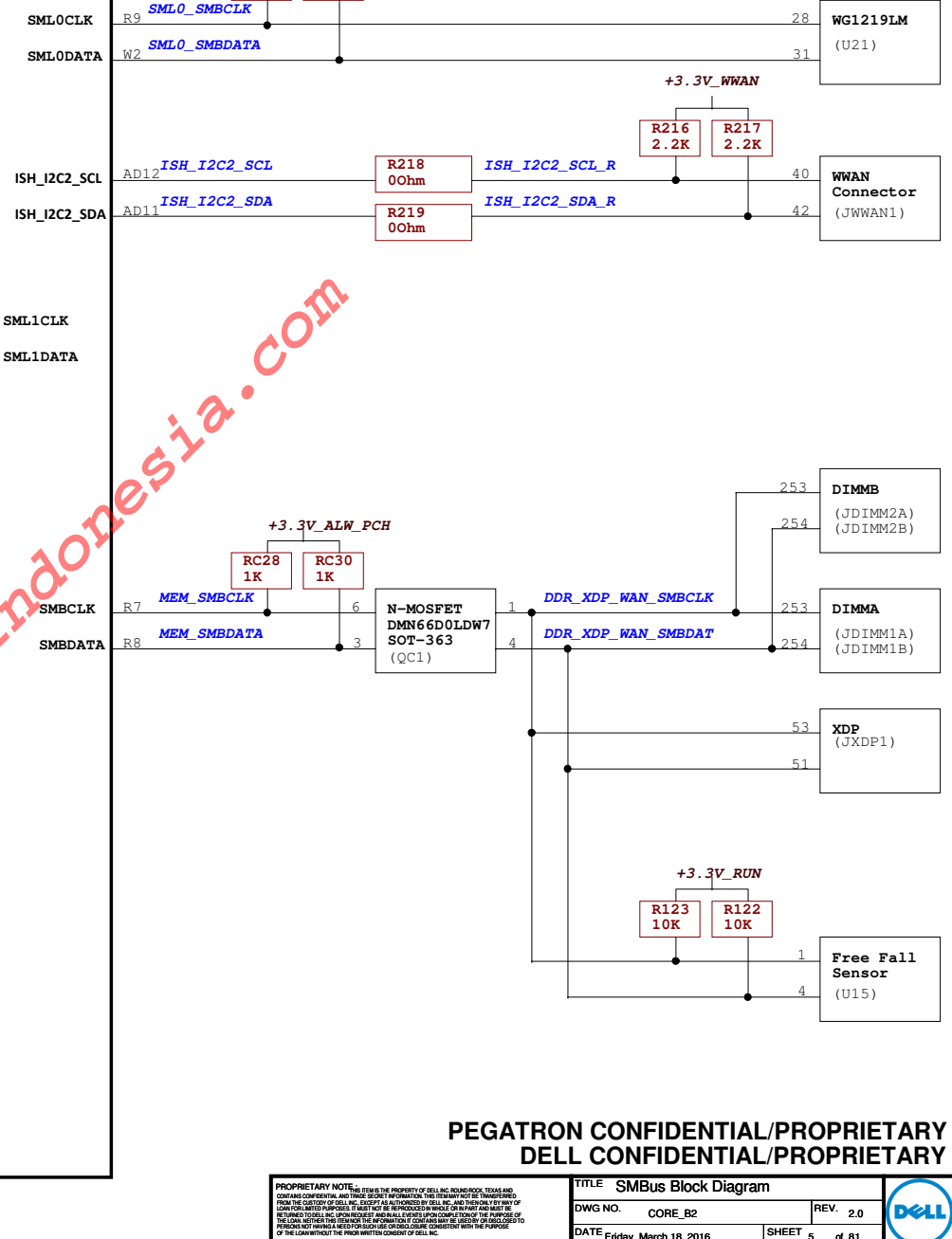


CORE_B2 SMBus Block Diagram (A00)

KBC MEC 5085

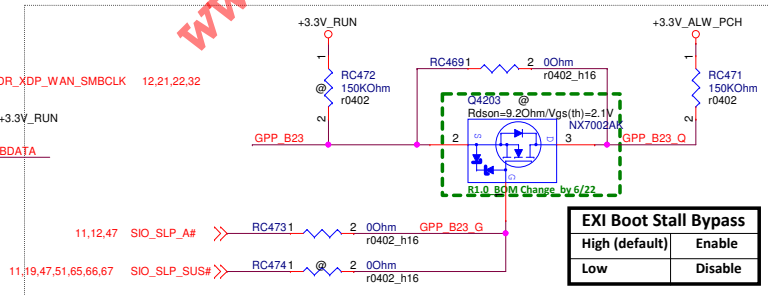
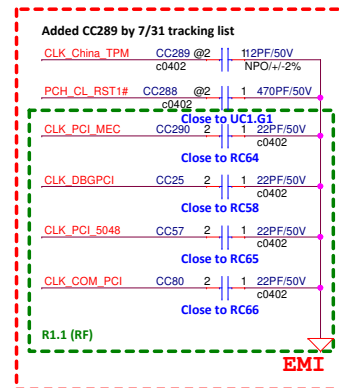
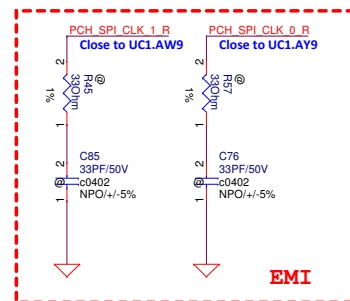
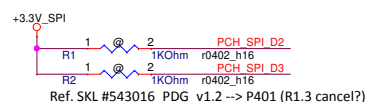
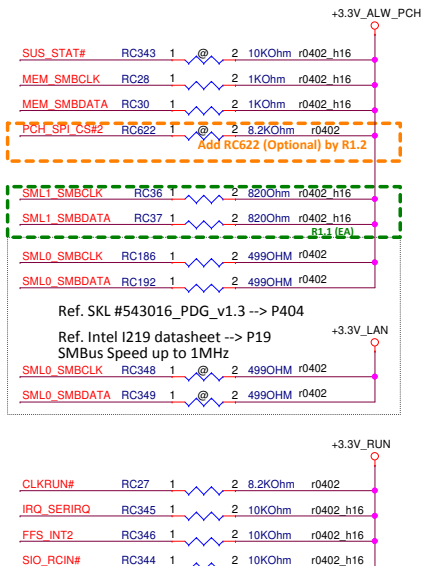


PCH UC1G




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DWG NO. CORE_B2	REV. 2.0		
DATE Friday, March 18, 2016	SHEET 5 of 81		

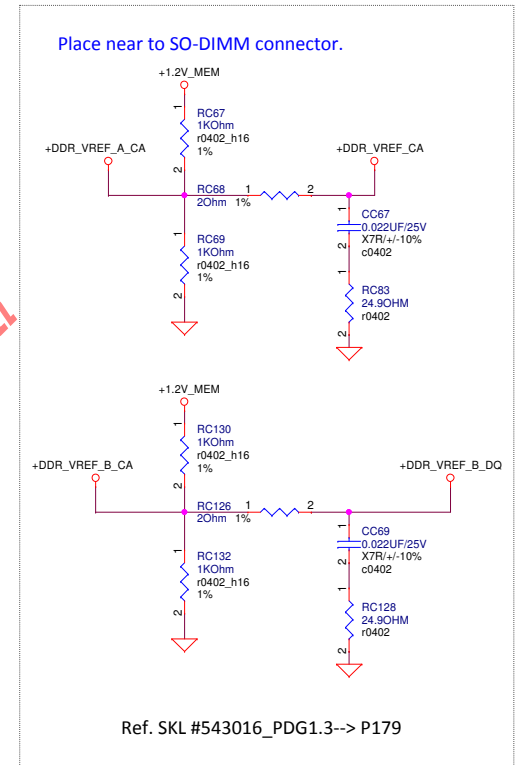
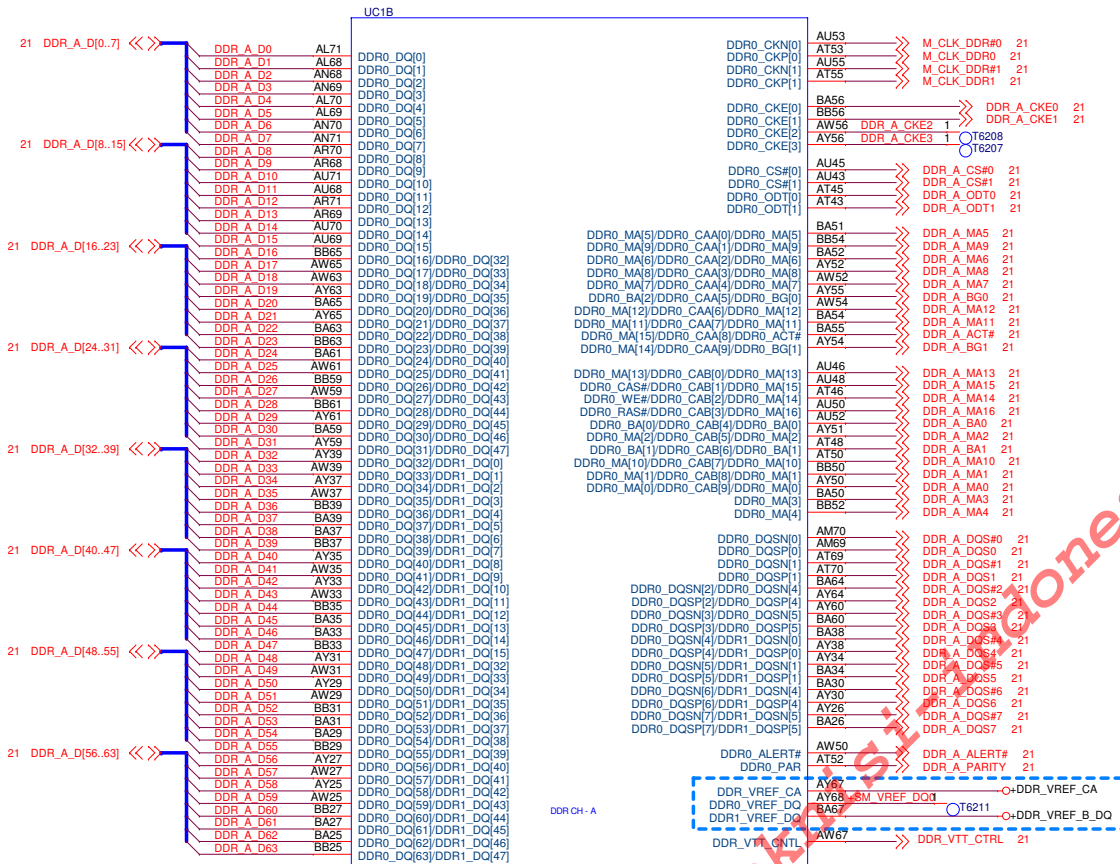


EC Interface	
High	ESPI
Low (default)	LPC

TITLE CPU_02 SPI/LPC/SMBus		
DWG NO. CORE_B2	REV. 2.0	
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DDR Interleave routing

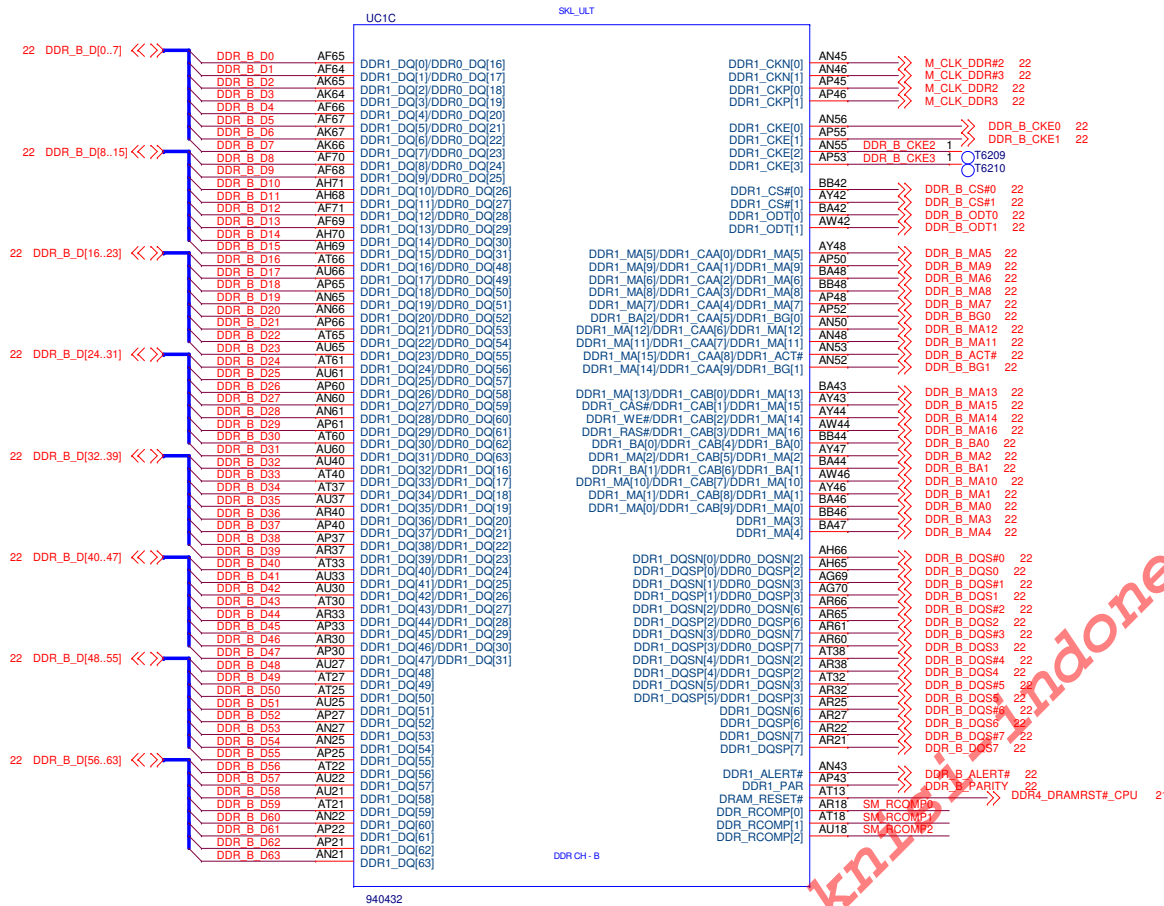


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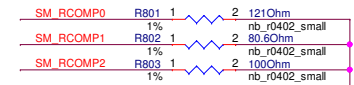
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DWG NO. CORE_B2		REV. 2.0	
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DDR interleave routing



DDR4 COMPENSATION SIGNALS



Layout Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

Ref. SKL #543016_PDG1.3--> P151

Interleaved Memory

Ref. SKL #544924_EDS_v0.95--> P32

IL		IL	
Channel	Byte	Channel	Byte
DDR0	Byte0	DDR1	Byte0
DDR0	Byte1	DDR1	Byte1
DDR0	Byte2	DDR1	Byte2
DDR0	Byte3	DDR1	Byte3
DDR0	Byte4	DDR1	Byte4
DDR0	Byte5	DDR1	Byte5
DDR0	Byte6	DDR1	Byte6
DDR0	Byte7	DDR1	Byte7

NIL		NIL	
Channel	Byte	Channel	Byte
DDR0	Byte0	DDR0	Byte2
DDR0	Byte1	DDR0	Byte3
DDR0	Byte4	DDR0	Byte6
DDR0	Byte5	DDR0	Byte7
DDR1	Byte0	DDR1	Byte2
DDR1	Byte1	DDR1	Byte3
DDR1	Byte4	DDR1	Byte6
DDR1	Byte5	DDR1	Byte7

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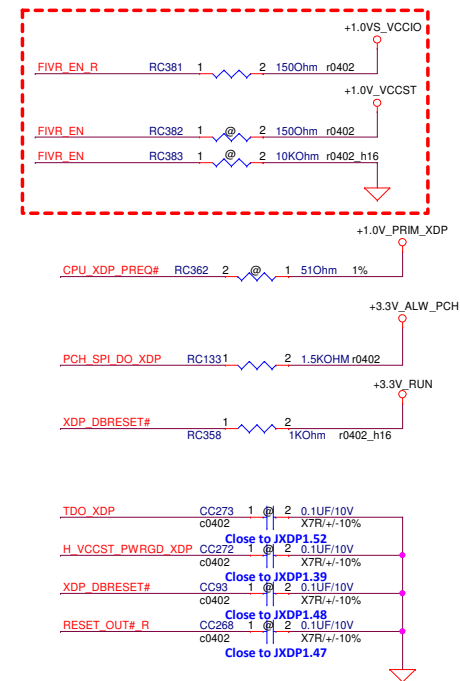
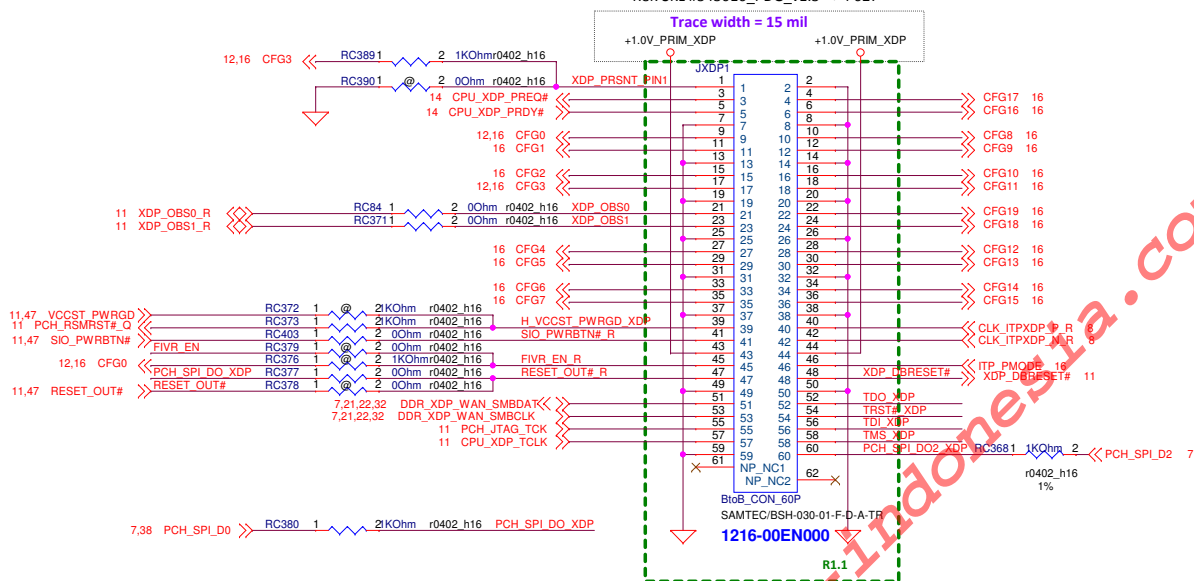
TITLE CPU_05 DDR4 Channel 1		
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Diagram illustrating the PCB layout for the JXP1 connector. The layout shows the connection of the JXP1 connector pins to the power planes. The connector pins are labeled 1 and 2, with a pitch of 1mm. The layout includes a 15 mil trace width and a 1mm pitch. The layout also shows the placement of the JXP1 connector near the JXP1 connector.

Ref. SKL #543016 PDG v1.3 --> P627



Pin connection diagram for JAPS1 connector. The diagram shows a 20-pin connector with pins numbered 1 to 20. Pins 1-10 are labeled 'SIDE1' and pins 11-20 are labeled 'SIDE2'. The connector is connected to a microcontroller pin header labeled 'FPC_CON_18P'. The connections are as follows:

Pin	Signal
1	+3.3V_ALW_PCH
2	SIO_SLP_S3#
3	+3.3V_ALW_DSW
4	SIO_SLP_S5#
5	SIO_SLP_S4#
6	SIO_SLP_A#
7	+3.3V_ALW_DSW
8	PCH_RTCRST#
9	
10	
11	POWER_SW#_MB
12	
13	SYS_RESET#
14	SIO_SLP_S0#
15	
16	
17	
18	
19	
20	

Ref. SKL #543016 PGD v1.3 --> P446

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TITLE CPU_07 JAPS1/JXDP1	
DWG NO. CORE_B2	REV. 2.0
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GFX

WLAN

EC/PC

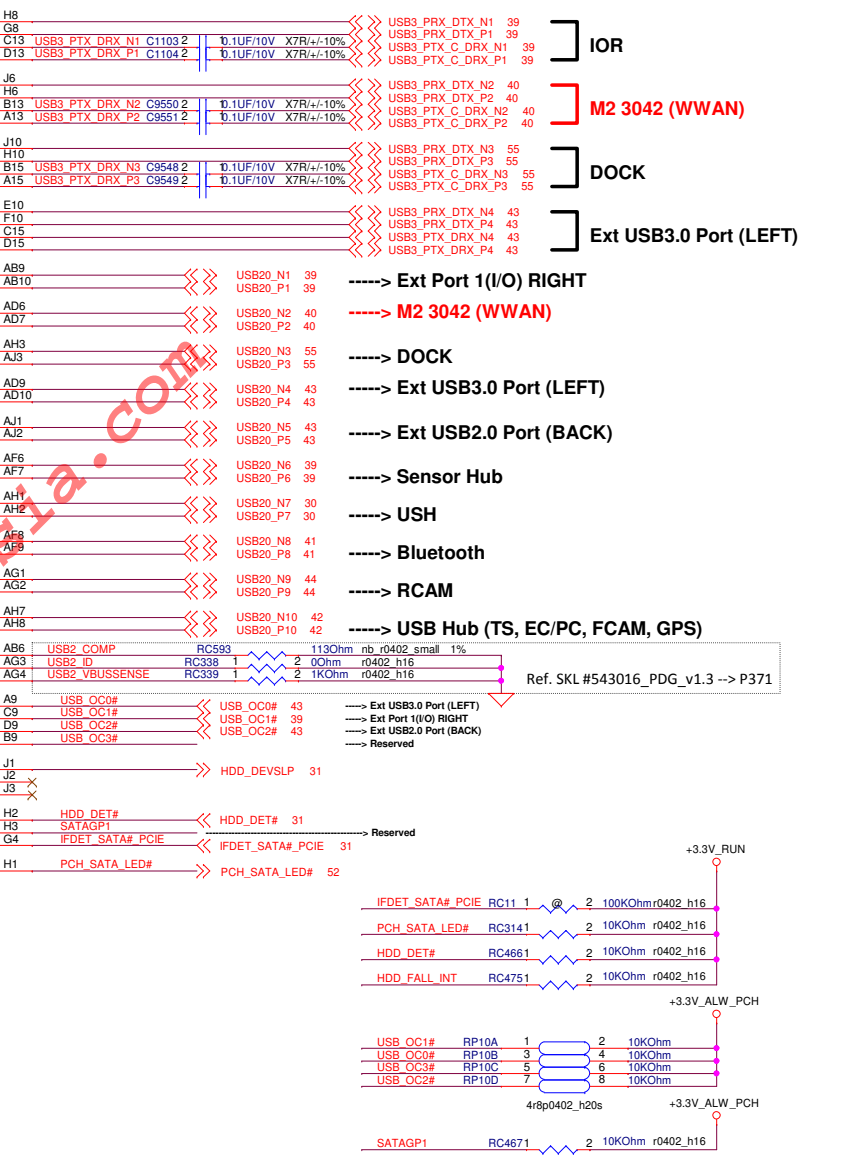
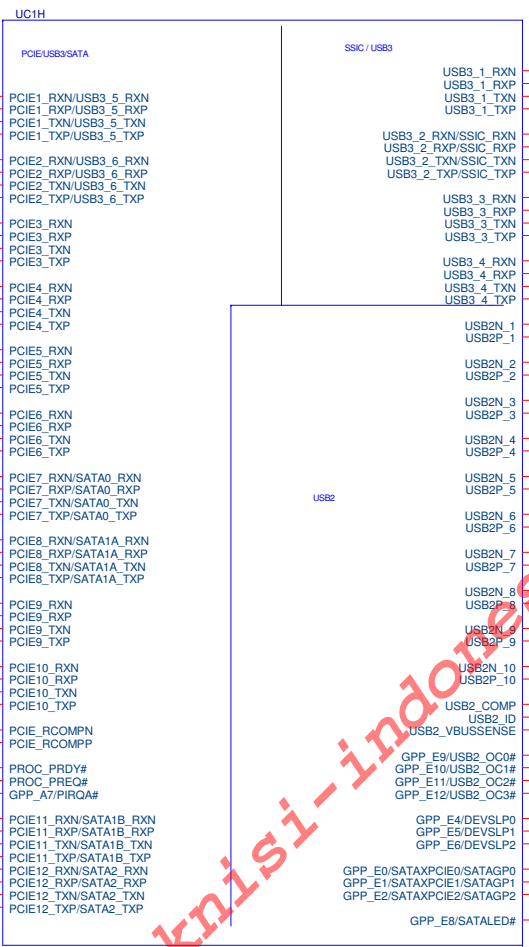
ODD

N/A

LOM

WWAN

SATA Express HDD



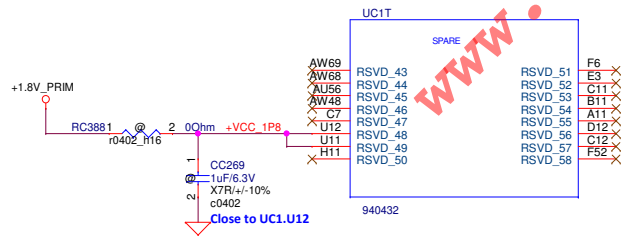
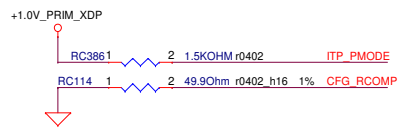
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PEG Training	
CFG7	1 : PEG train immediately following RESET# de assertion. (default) 0 : PEG wait BIOS for training.



Pin-to-pin comparison diagram for Cannonlake and Skylake processors. The diagram shows two columns of pins, one for Cannonlake (left) and one for Skylake (right), with their respective functions. A central column lists reserved signals. The diagram includes various signal types like configuration (CFG), reserved signals (RSVD), and power management (PMP). A large red watermark "Si-indonesia.com" is overlaid diagonally across the center.

Left Column (Cannonlake):

- 12 CFG0
- 12 CFG1
- 12 CFG2
- 12 CFG3
- 12 CFG4
- 12 CFG5
- 12 CFG6
- 12 CFG7
- 12 CFG8
- 12 CFG9
- 12 CFG10
- 12 CFG11
- 12 CFG12
- 12 CFG13
- 12 CFG14
- 12 CFG15
- 12 CFG16
- 12 CFG17
- 12 CFG18
- 12 CFG19
- CFG_RCOMP
- ITP_PMODE
- AY2
- AY1
- D1
- D3
- K46
- K45
- AL25
- AL27
- C71
- B70
- F60
- A52
- T7110
- T7120
- J71
- J68
- F65
- G65
- F61
- E61

Right Column (Skylake):

- B668
- B669
- AK13
- AK12
- BB2
- BA3
- AU5
- AT5
- D5
- D4
- B2
- C2
- B3
- A3
- AW1
- E1
- E2
- BA4
- BB4
- A4
- C4
- BB5
- A69
- B69
- AY3
- D71
- C70
- C54
- D54
- AY4
- BB3
- AY71
- AR56
- AW71
- AW70
- AP56
- C64
- PROC_SELECT#

Central Column (Reserved Signals):

- RESERVED SIGNALS-1
- CFG[0]
- CFG[1]
- D65
- CFG[2]
- CFG[3]
- CFG[4]
- CFG[5]
- CFG[6]
- CFG[7]
- CFG[8]
- CFG[9]
- CFG[10]
- CFG[11]
- CFG[12]
- CFG[13]
- CFG[14]
- CFG[15]
- CFG[16]
- CFG[17]
- CFG[18]
- CFG[19]
- CFG_RCOMP
- ITP_PMODE
- RSVD_5
- RSVD_6
- RSVD_7
- RSVD_8
- RSVD_9
- RSVD_10
- RSVD_11
- RSVD_12
- RSVD_13
- RSVD_14
- RSVD_15
- RSVD_16
- RSVD_TP_1
- RSVD_TP_2
- RSVD_17
- RSVD_18
- VSS_360
- VSS_361
- RSVD_19
- RSVD_20

Bottom Right Note:

Pop: for Cannonlake
De-pop: for Skylake

1.0V_VCCST

2 100kOhm

0402_h16

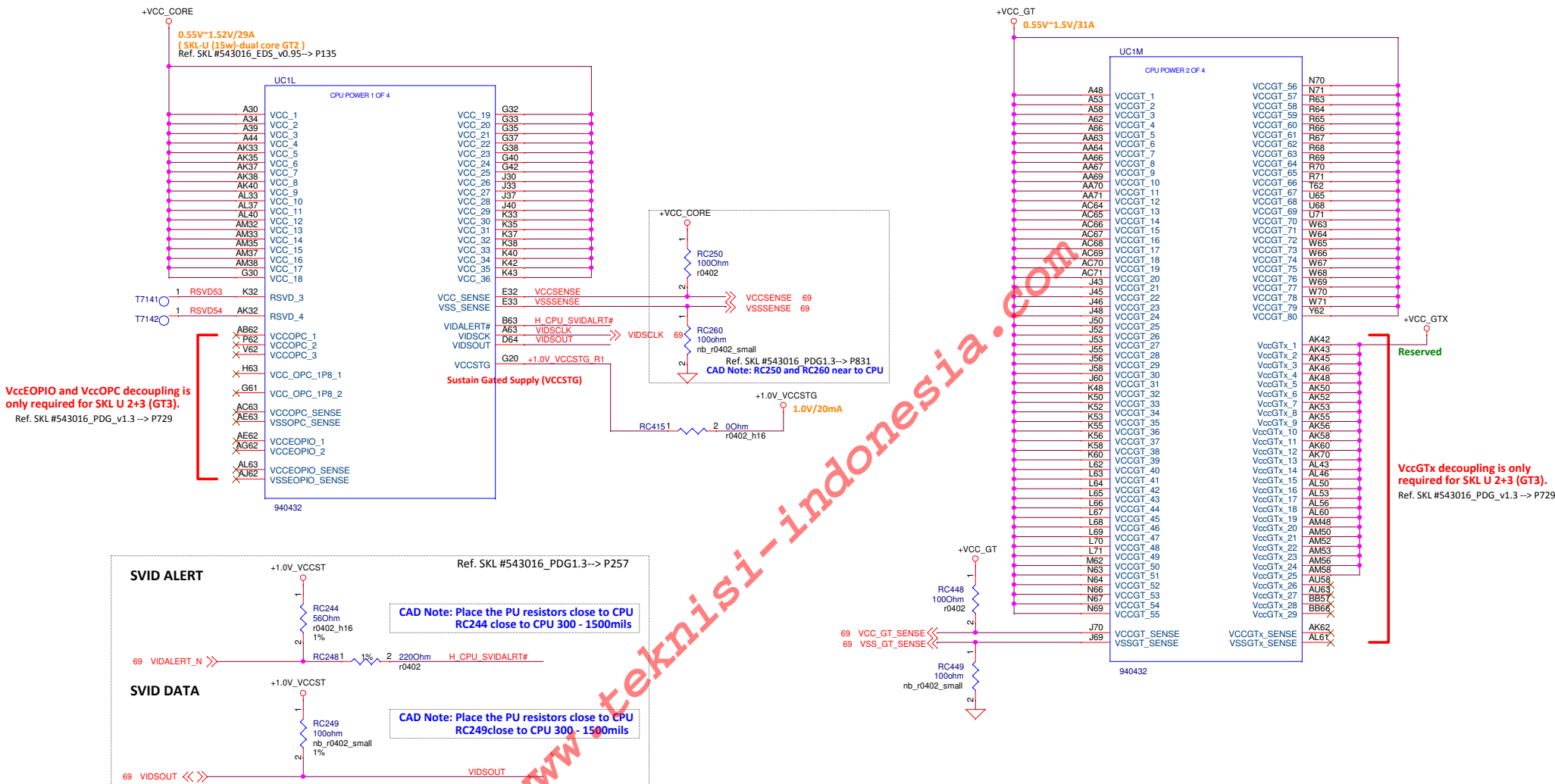
Pop: for Cannonlake
De-pop: for Skylake

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TITLE CPU_11 CFG/RSVD		
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DATE	Friday, March 18, 2016	SHEET 16 of 81



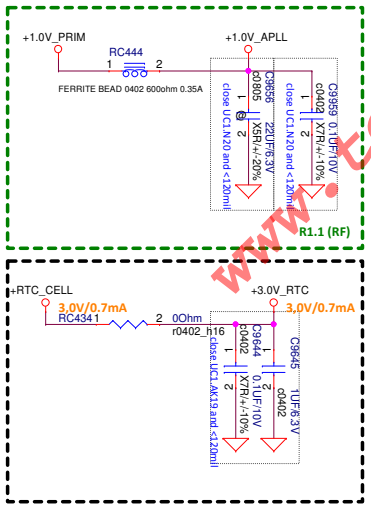
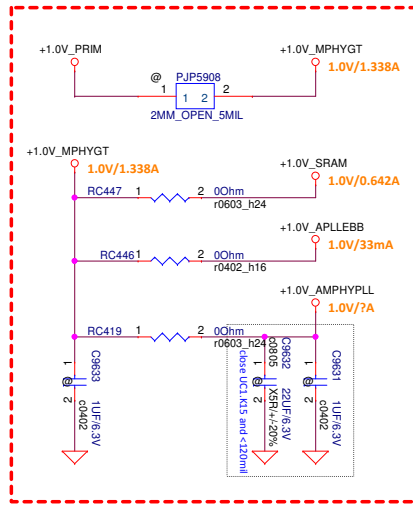
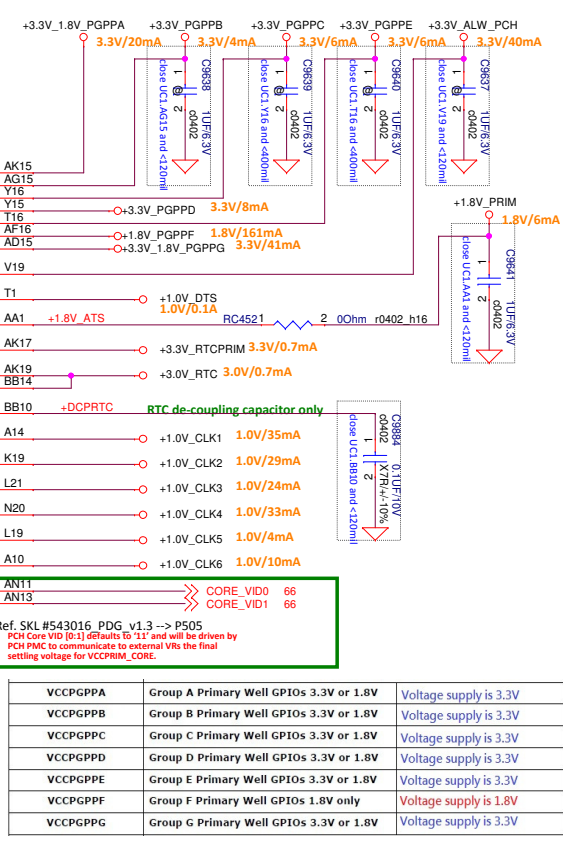
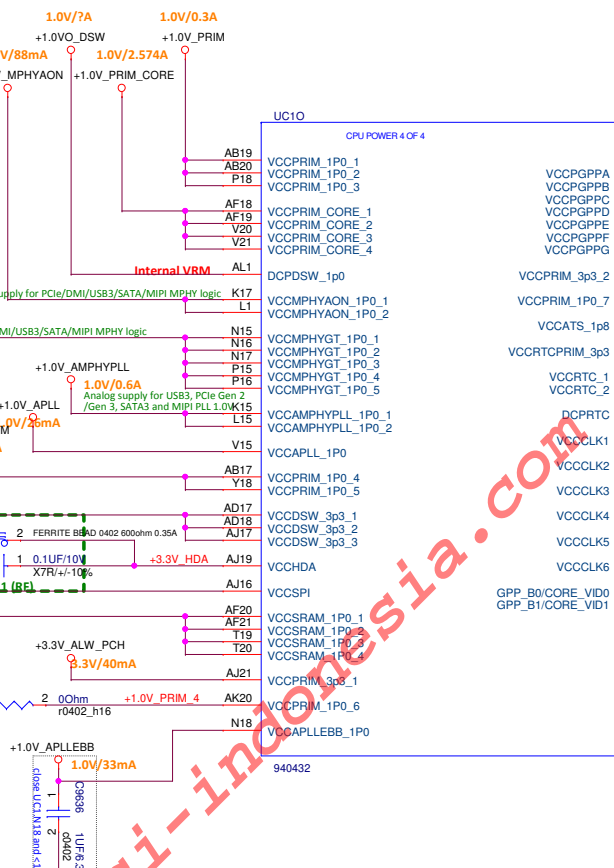
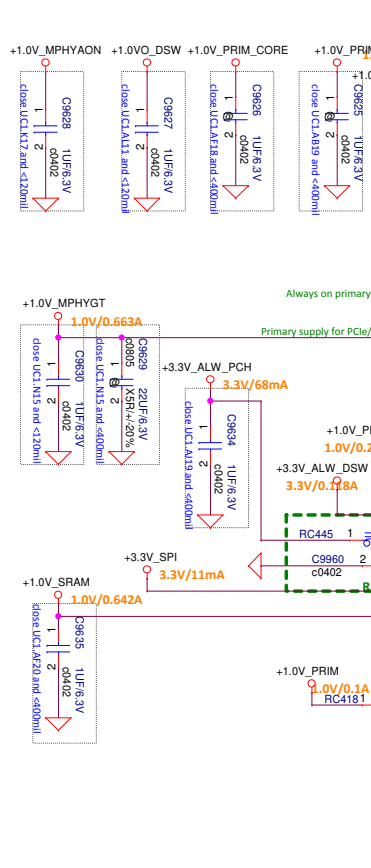
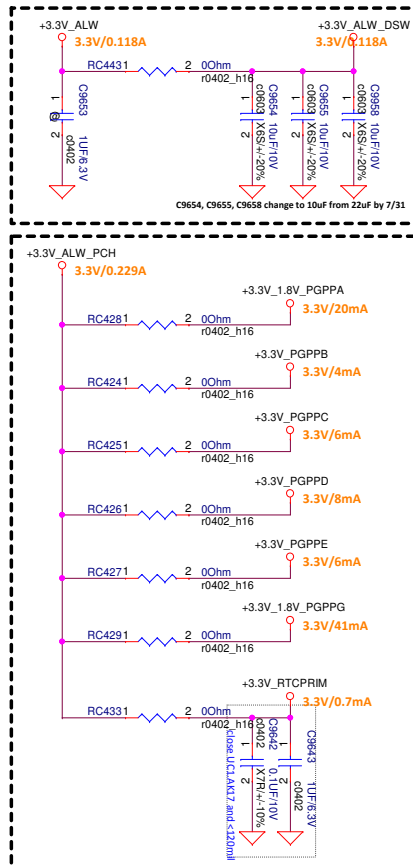


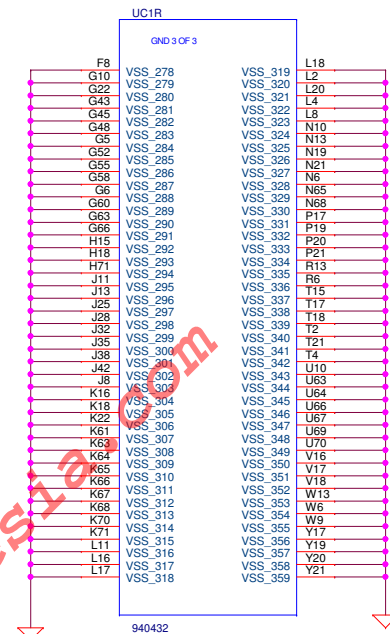
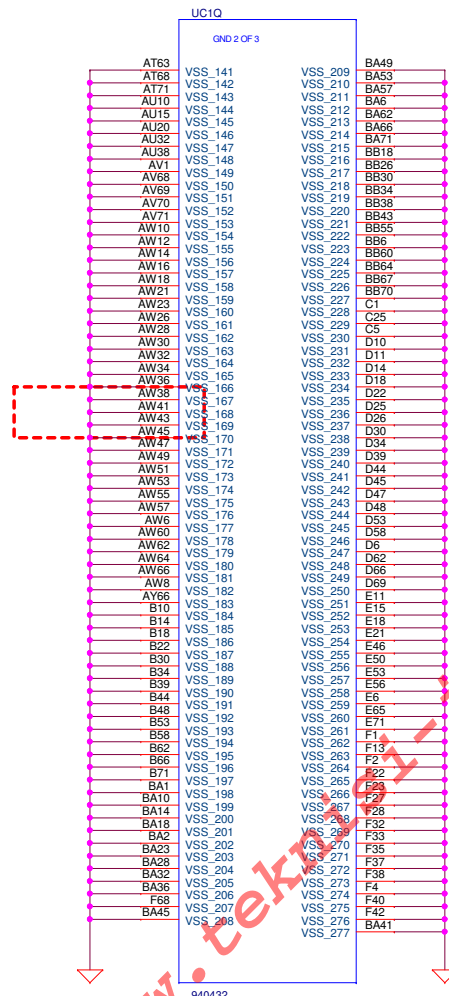
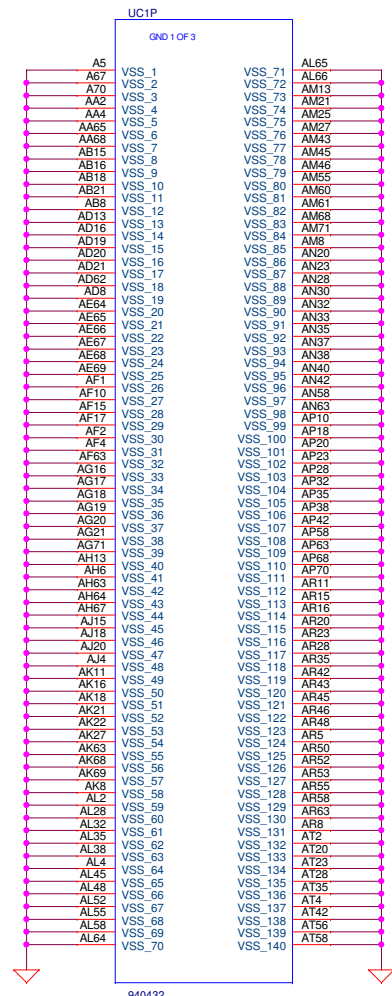
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TITLE	CPU_12 Power Group 1	
DWG NO.	CORE_B2	REV. 2.0
DATE	Friday, March 18, 2016	SHEET 17 of 81







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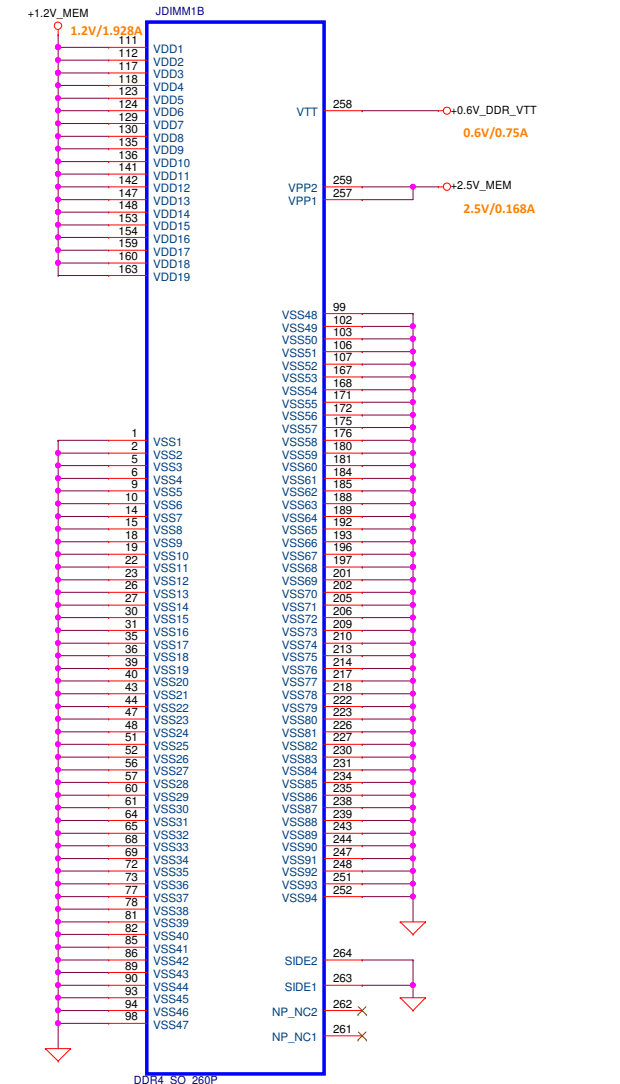
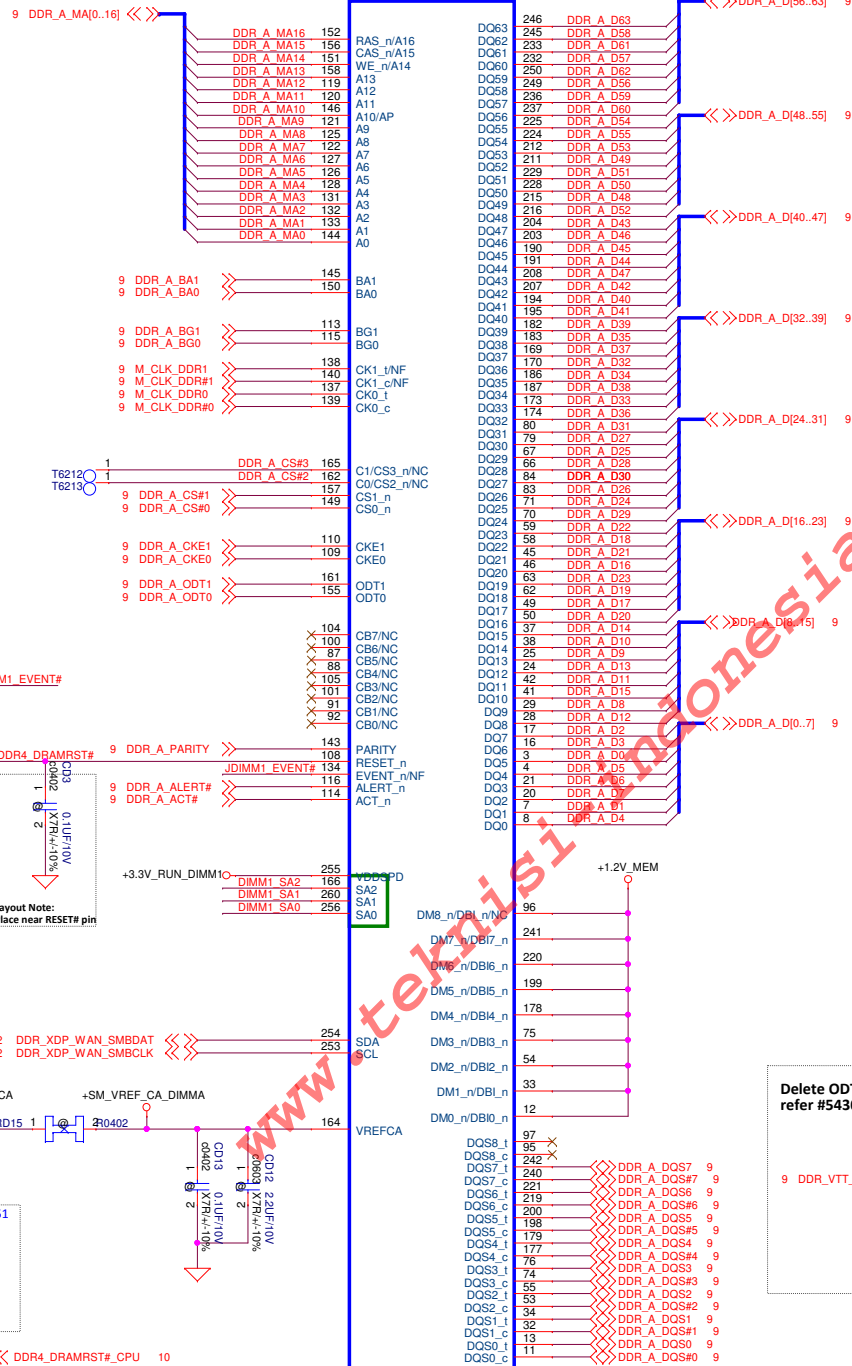
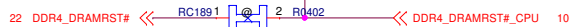
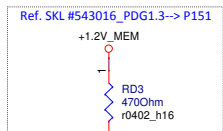
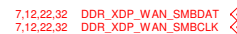
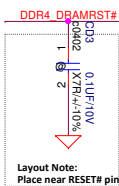
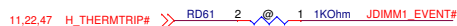
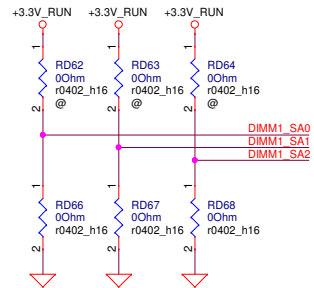
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TITLE CPU_15 VSS (GND)		
DWG NO.	CORE_B2	REV. 2.0
DATE	Friday, March 18, 2016	SHEET 20 of 81

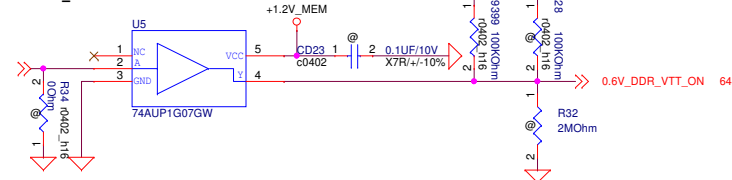


(I2C slave address select for SPD)

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0




Delete ODT Genertation, connect directly to CPU
refer #543016 SKL-U PDG v1.3 --> P174



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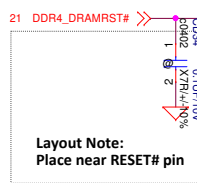
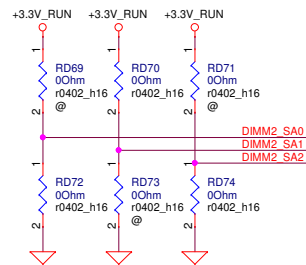
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TITLE		DDR4 JDIMM1		
DWG NO.	CORE_B2	REV.	2.0	
DATE	Friday, March 18, 2016	SHEET	21 of 81	

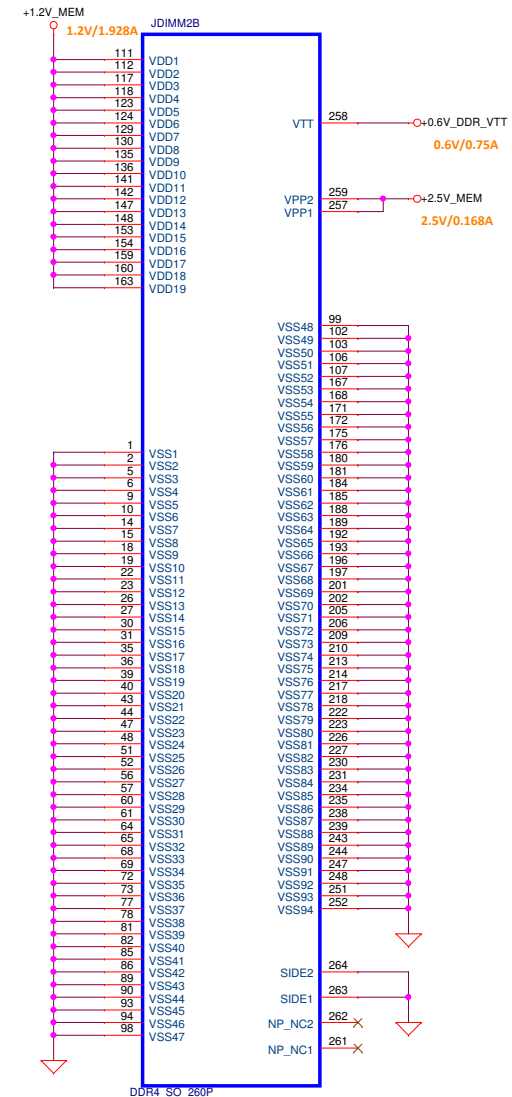
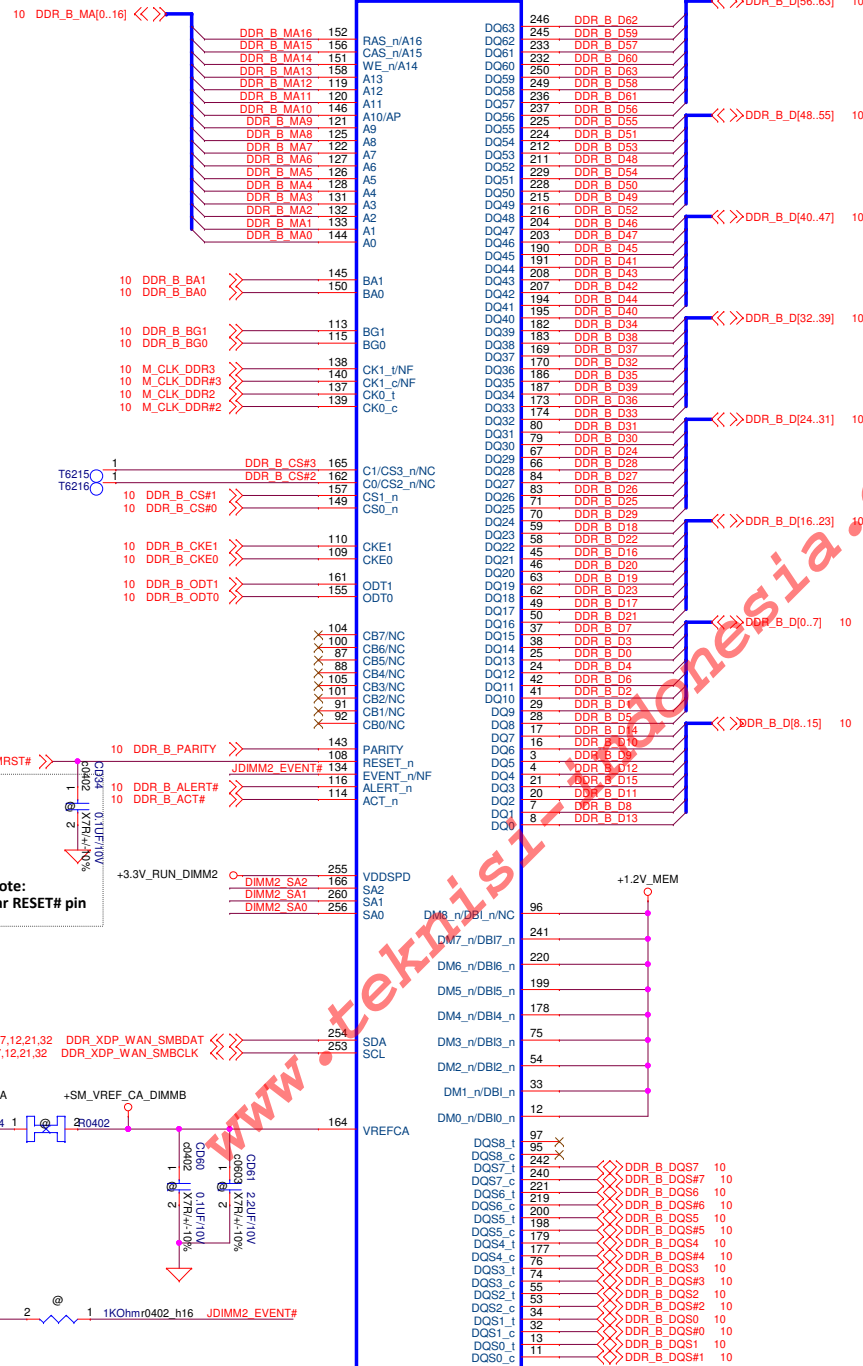
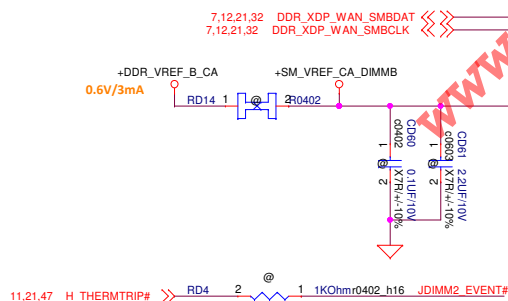


(I2C slave address select for SPD)

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0




Layout Note:
Place near RE



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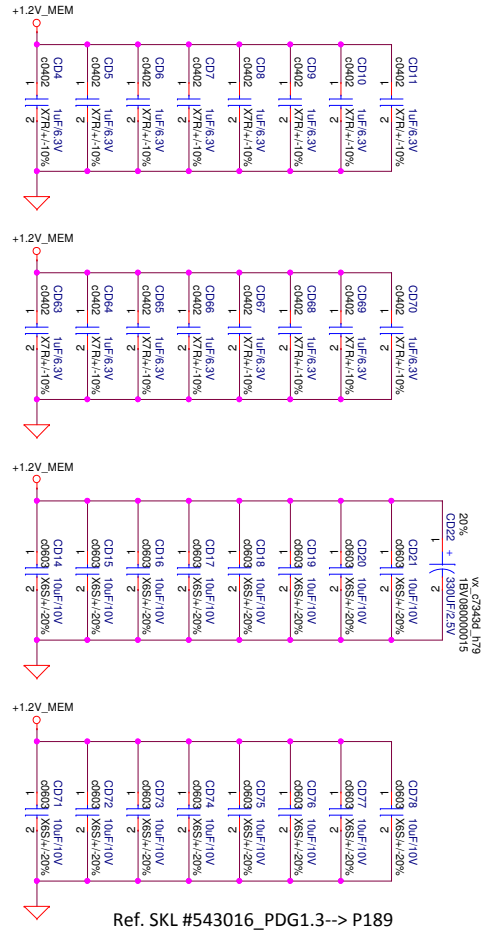
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TITLE		DDR4 JDIMM2		
DWG NO.		CORE_B2	REV. 2.0	
DATE		Friday, March 18, 2016	SHEET 22 of 81	

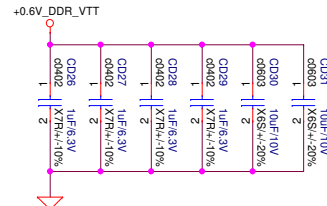


DDR4 DIMM1

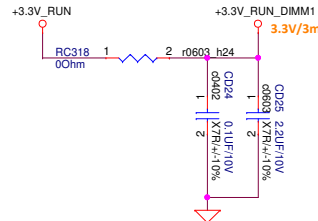
Layout Note:
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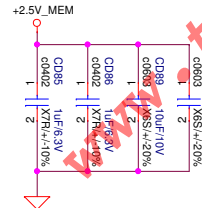
Layout Note:
Place near JDIMM1.258



Layout Note:
Place near JDIMM1.255



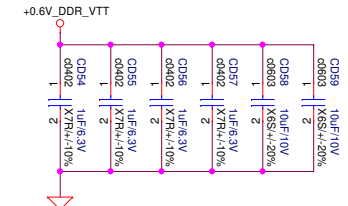
Layout Note:
Place near JDIMM1.257,259



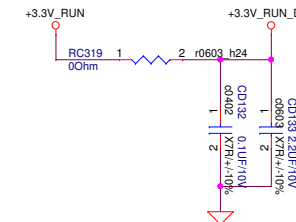
Ref. SKL #543016_PDG1.3--> P189

DDR4 DIMM2

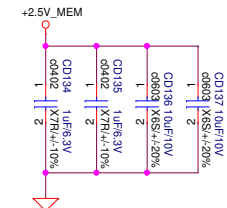
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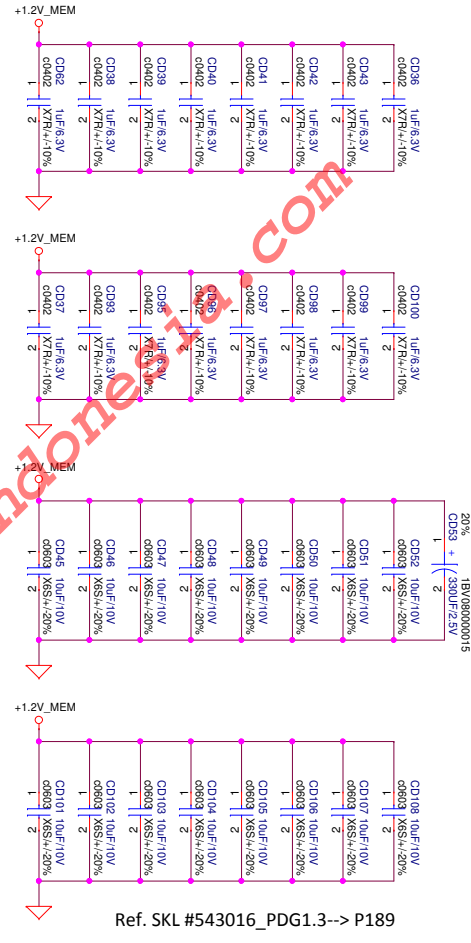
Layout Note:
Place near JDIMM2.255



Layout Note:
Place near JDIMM2.257,259




Layout Note:
Place near JDIMM2



Ref. SKL #543016_PDG1.3--> P189

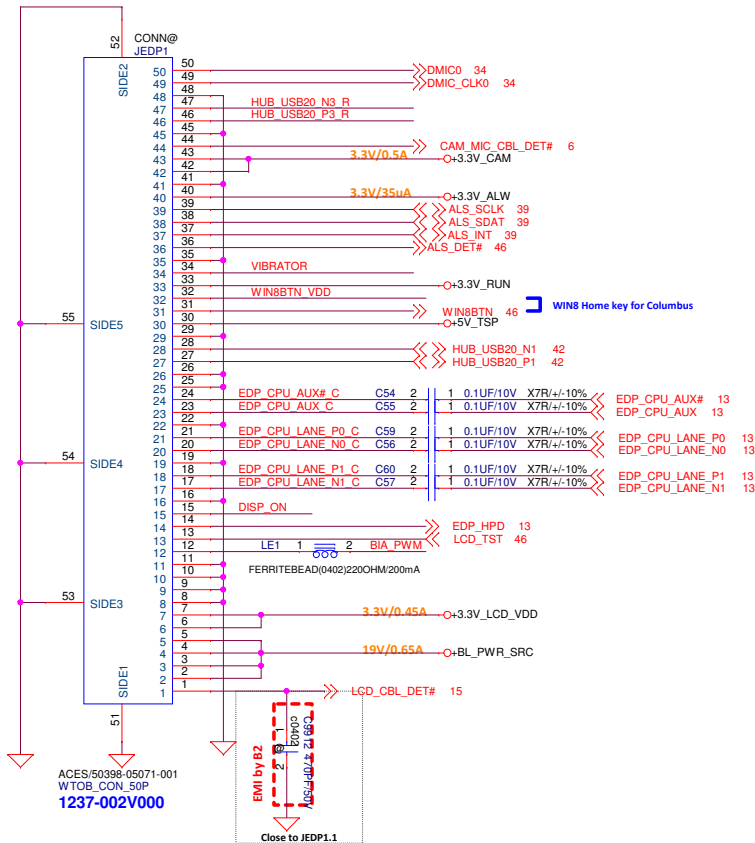
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TITLE DDR4 JDIMM Decoupling		
DWG NO. CORE_B2	REV. 2.0	
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eDP Connector



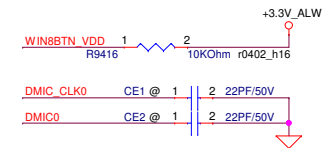
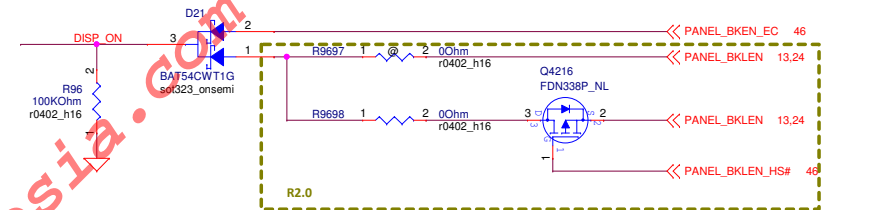
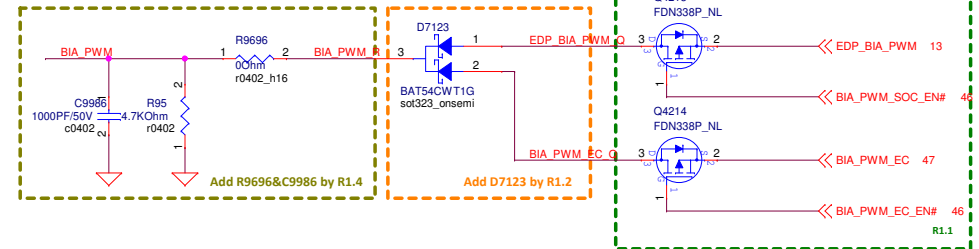
--> CAM+DMIC

--> ALS

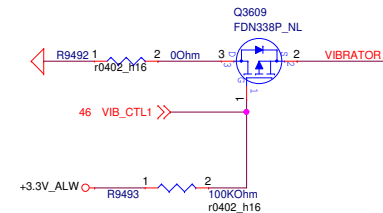
--> Vibrator

--> Touch Screen

--> eDP Panel



Vibrator Control



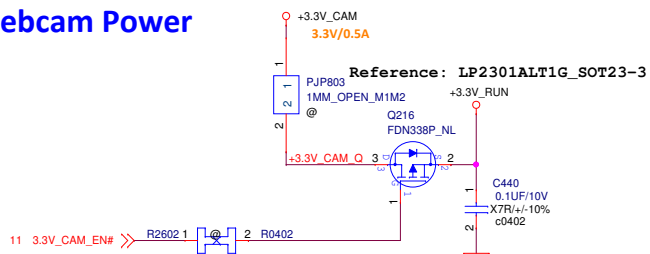
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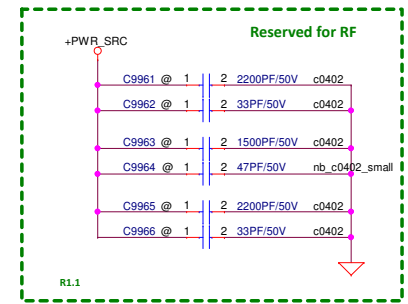
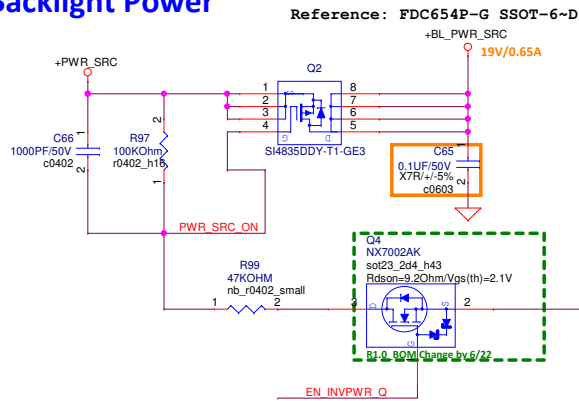
TITLE	JEDP1
DWG NO.	CORE_B2
REV.	2.0
DATE	Friday, March 18, 2016
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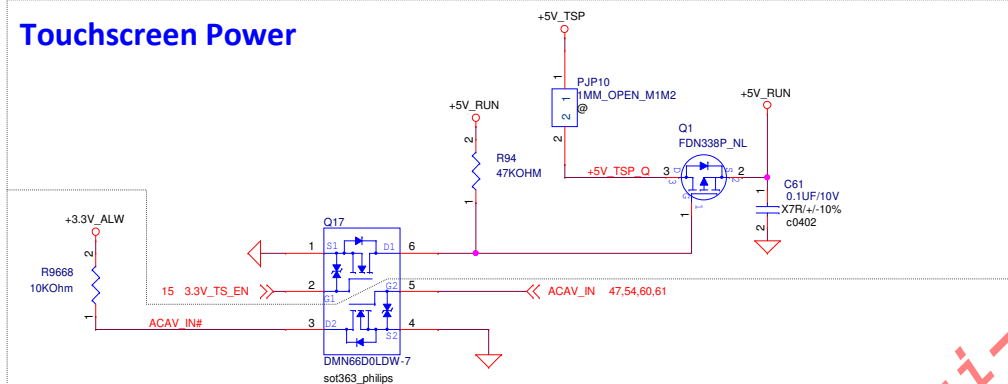
Webcam Power



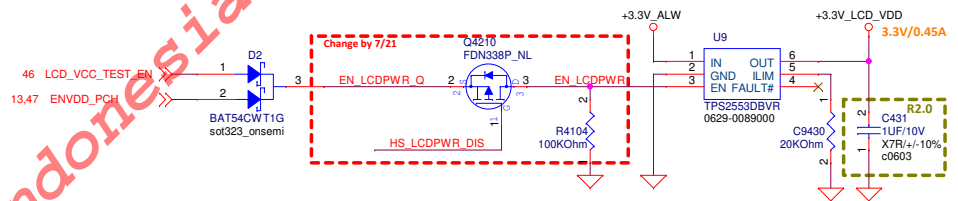
Backlight Power



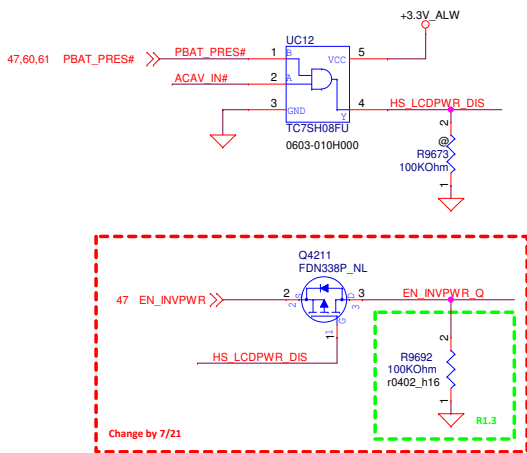
Touchscreen Power



LCDVDD Power



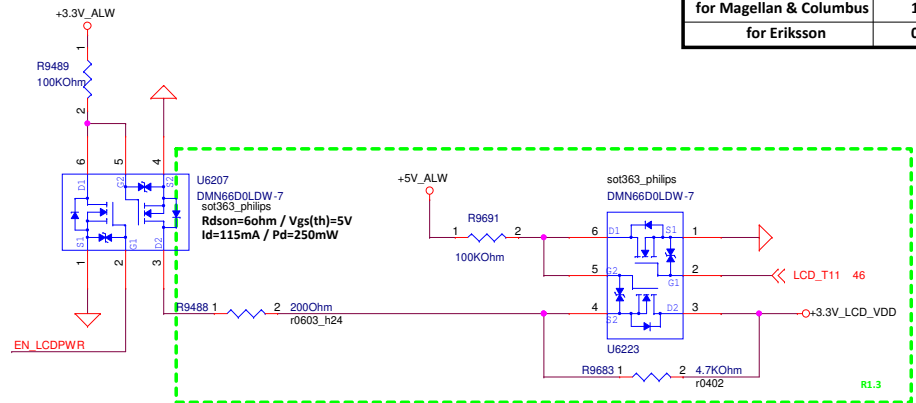
LCD Turn Off for Hotswap



Battery (PBAT_PRES#)	AC IN (ACAV_IN#)	AND logic (HS_LCDPWR_DIS)	Panel Power
L	L	L	ON
L	H	L	ON
H	L	L	ON
H	H	H	OFF

Note: Battery(PBAT_PRES#),ACIN(ACAV_IN#)
H= un-plug, L= plug

LCDVDD Discharge



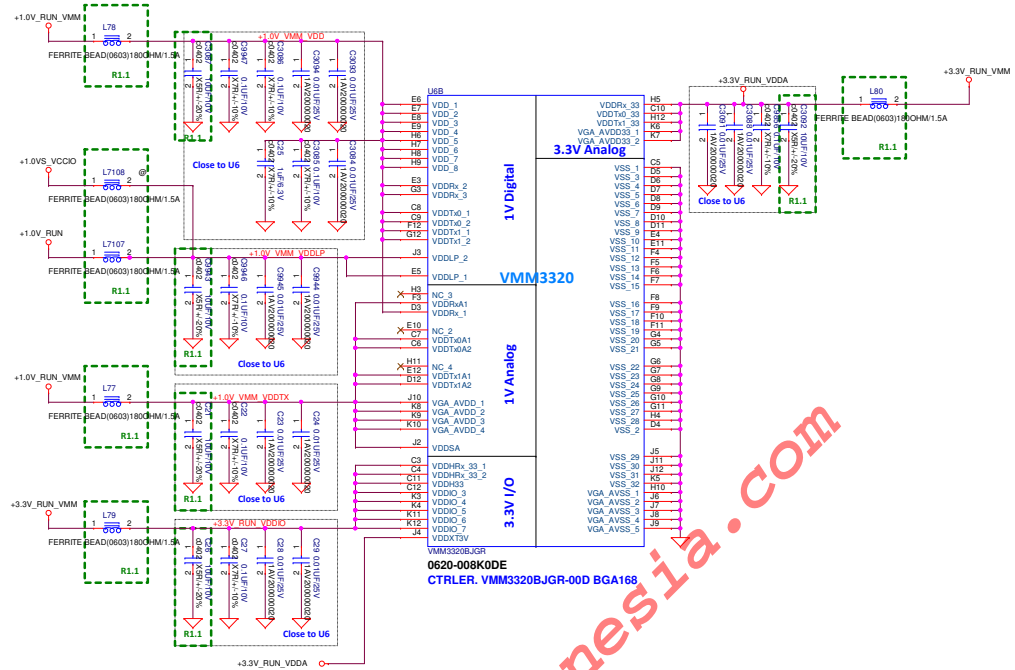
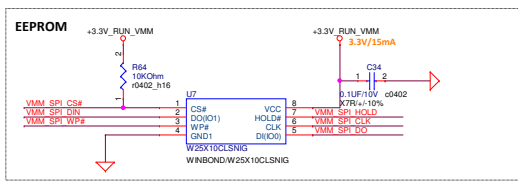
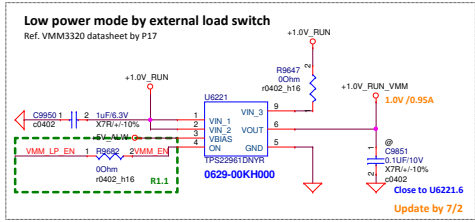
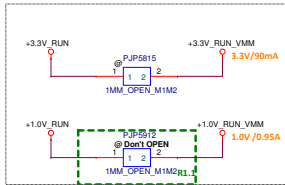
eDP power down timing at T11	
Function	LCD_T11
for Magellan & Columbus	1
for Eriksson	0

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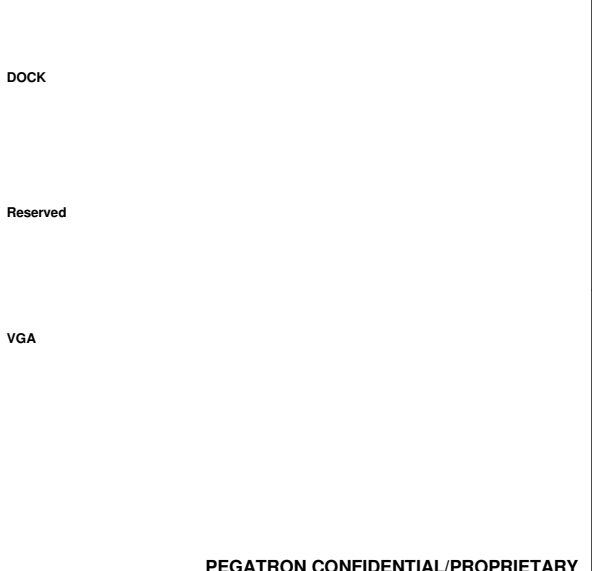
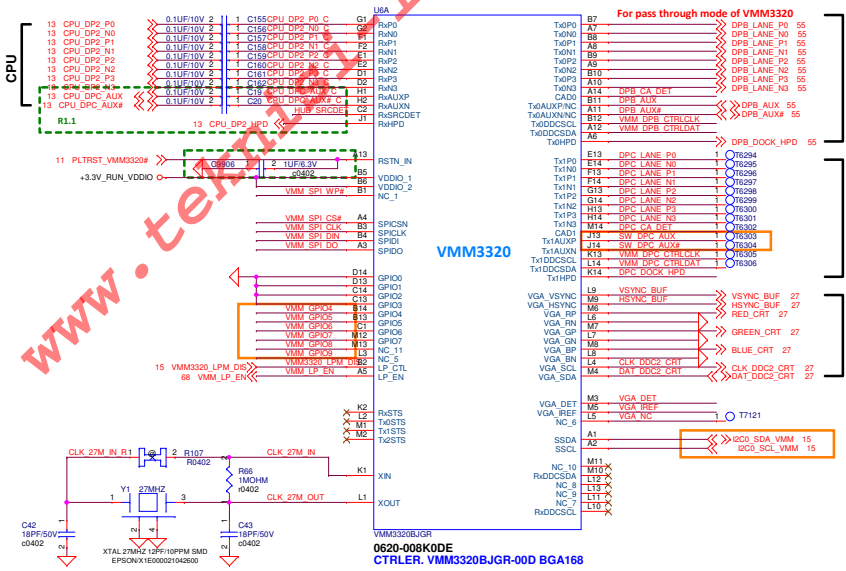
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TITLE JEDP1 Power	
DWG NO. CORE_B2	REV. 2.0
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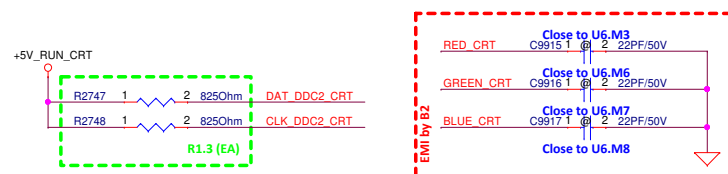
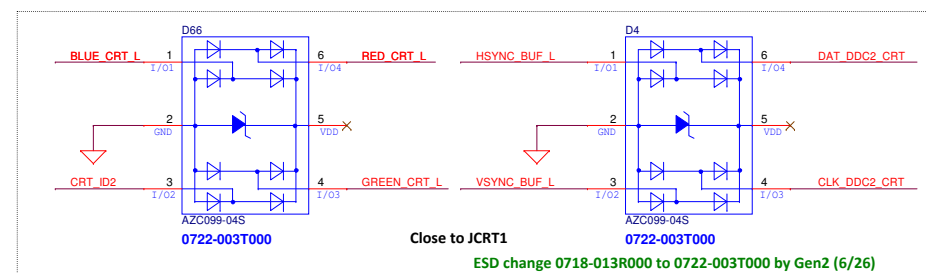
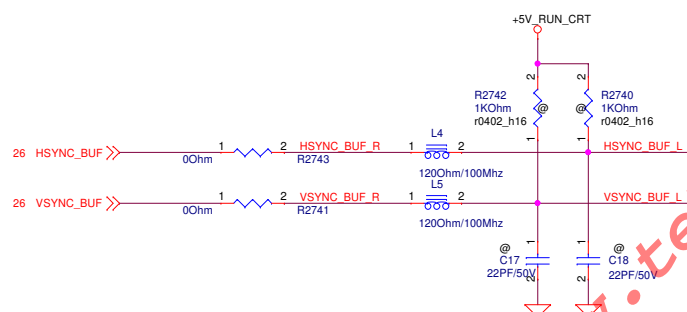
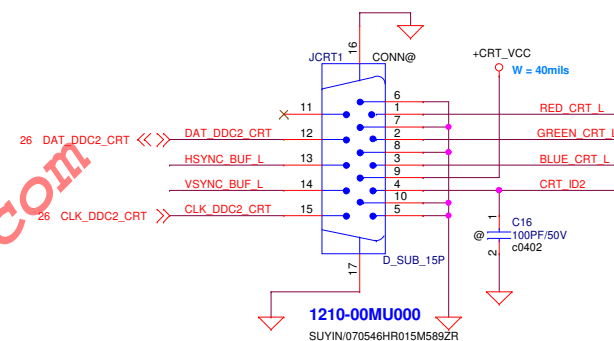
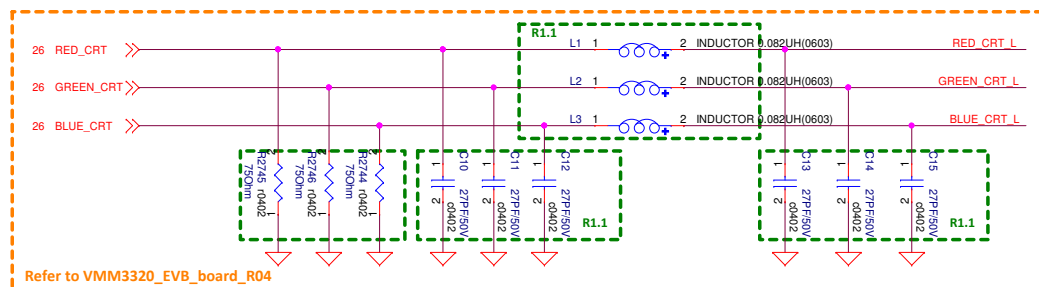


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VGA Connector



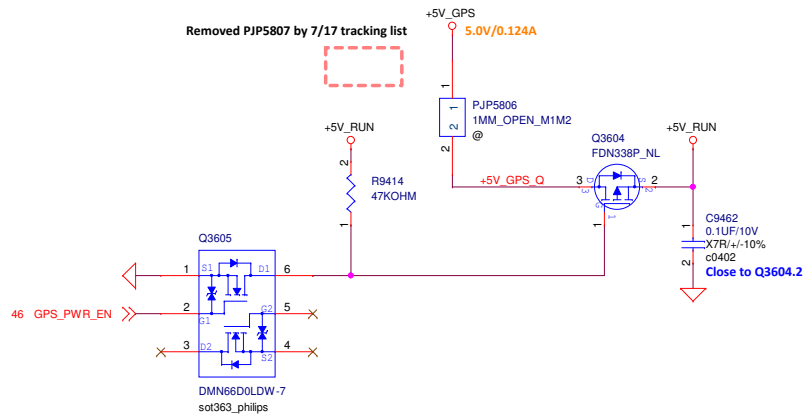
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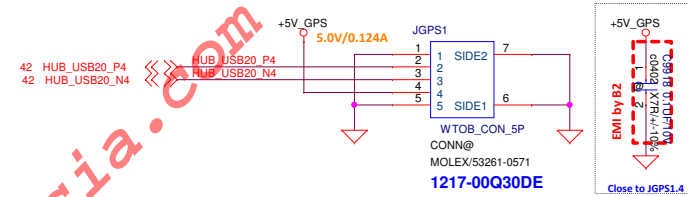
TITLE JCRT1	
DWG NO. CORE_B2	REV. 2.0
DATE Friday, March 18, 2016	SHEET 27 of 81




GPS Power

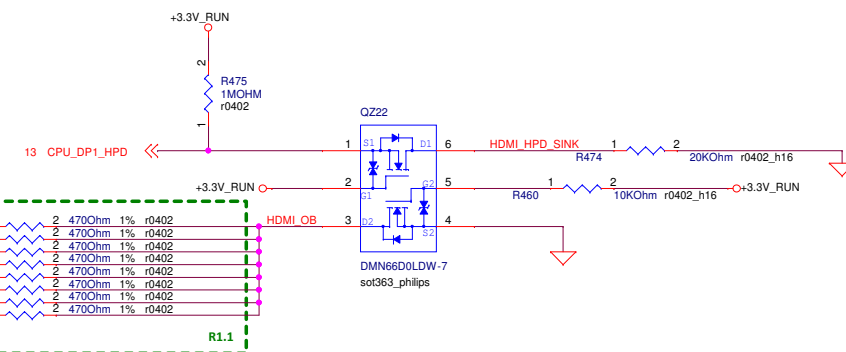
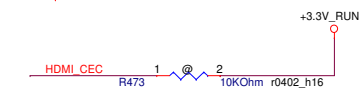
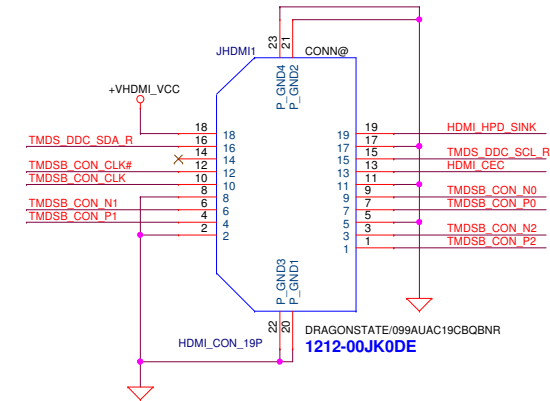
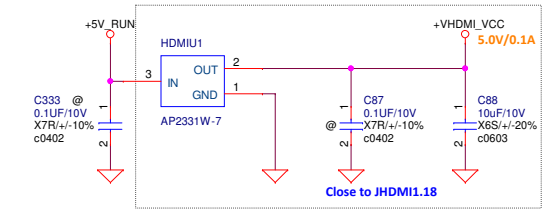
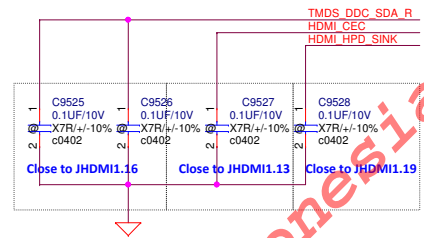
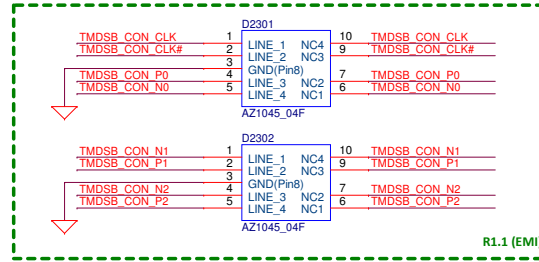
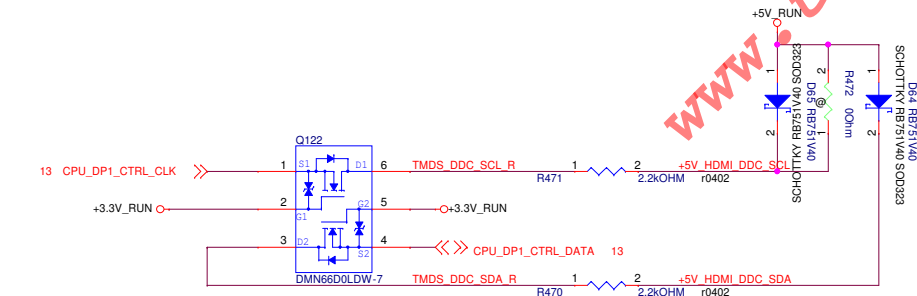
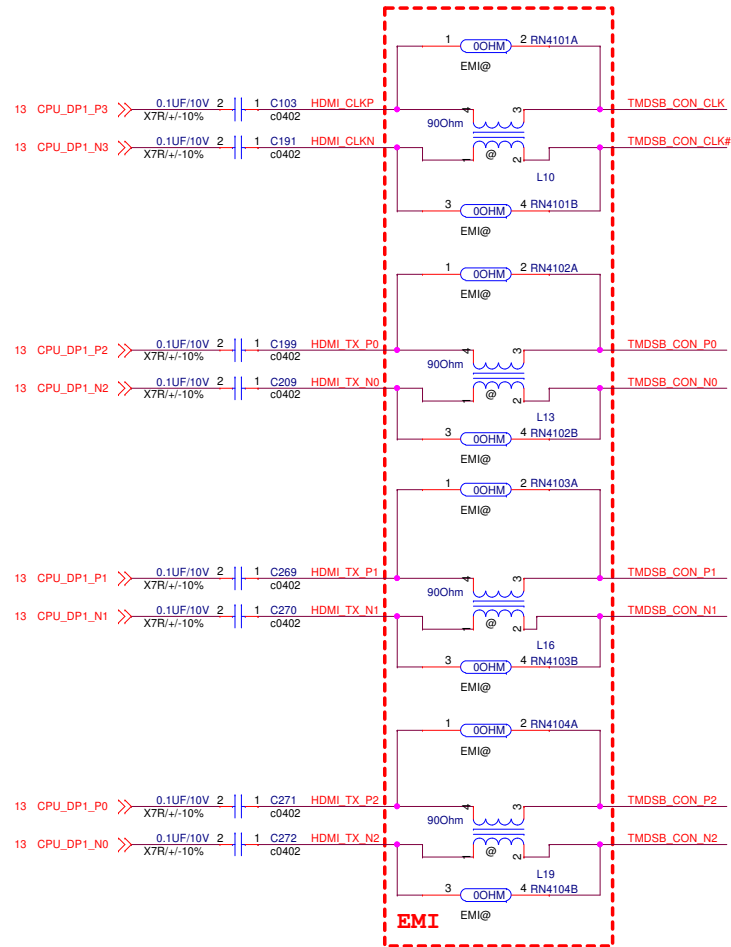


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DWG NO. CORE_B2		REV. 2.0		
DATE Friday, March 18, 2016		SHEET 28 of 81		



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DWG NO. CORE_B2	REV. 2.0		
DATE Friday, March 18, 2016	SHEET 29 of 81		

47 USH_SMBCLK
6 BCM5882_ALERT#
+3.3V_ALW
+5V_ALW2
+3.3V_RUN
41,42,45,49,54 PCI_PLTRST# AND CONTACTLESS_DET#

3.3V/0.8A
20 mils
3.3V/70mA

R9574 1 2 00hm +5V_ALW2_R
r0402_h16

11 11
13 13
15 15
17 17
19 19
21 21
23 23
25 25
29 29

9 9
11 11
13 13
14 14
16 16
18 18
20 20
22 22
24 24
26 26
30 30

US
r0

SIDE3 SIDE4
FPC_CON_86P
1218-02MA000

JSEC1 change 20P to 26P by Gen2

14 USB20_N7 <<>>
14 USB20_P7 <<>>

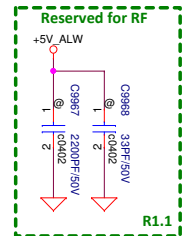
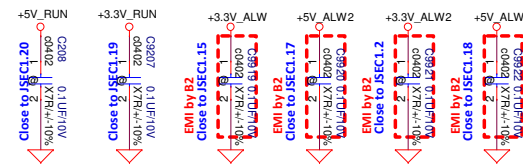
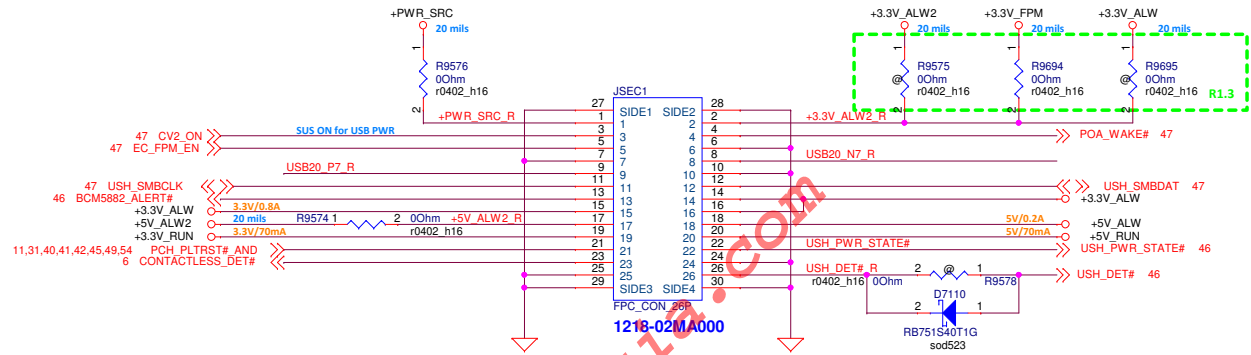
3 000H 4 RN4105B
900hm
1 000H 2 RN4105A

USB20_N7_R
USB20_P7_R

EMI

+5V_RUN
C808 0.1uF/10V
d0402 X7R/+10%
Close to JSEC1, 10
Close to JSEC1, 10

+3.3V_RUN
C807 0.1uF/10V
d0402 X7R/+10%
Close to JSEC1, 10
Close to JSEC1, 10



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SATA Express Re-Driver

PS8558B Note:

Equalizer control and program for channel A
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K
[A_EQ0,A_EQ1,A_EQ2] ==

L/L/L : for channel loss up to 17.3dB (default)
L/H/L : for channel loss up to 14.1dB
H/L/L : for channel loss up to 18.7dB
H/H/L : for channel loss up to 20.5dB
L/L/H : for channel loss up to 18dB
L/H/H : for channel loss up to 10dB
H/L/H : for channel loss up to 15.9dB
H/H/H : for channel loss up to 19.6dB

Equalizer control and program for channel B
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K
[B_EQ0,B_EQ1,B_EQ2] ==

L/L/L : for channel loss up to 17.3dB (default)
L/H/L : for channel loss up to 14.1dB
H/L/L : for channel loss up to 18.7dB
H/H/L : for channel loss up to 20.5dB
L/L/H : for channel loss up to 18dB
L/H/H : for channel loss up to 10dB
H/L/H : for channel loss up to 15.9dB
H/H/H : for channel loss up to 19.6dB

Programmable output de-emphasis level setting for channel A.
A_DE0: internally pulled up at ~150K
A_DE1 internally pulled down at ~150K
[A_DE1,A_DE0] ==

L/L -2 dB
H/L -7.5dB
L/H -3.5dB (default)
H/H -6 dB

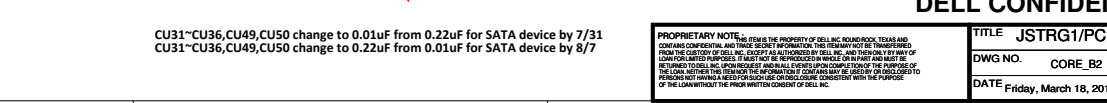
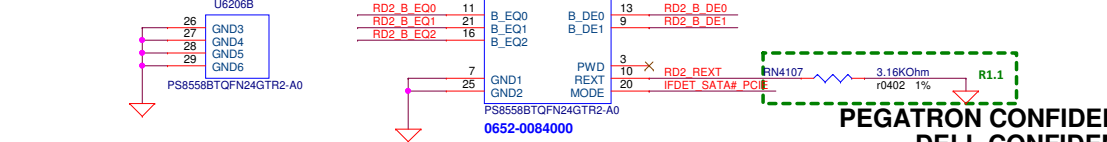
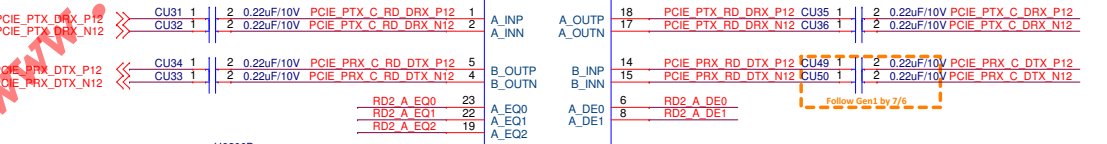
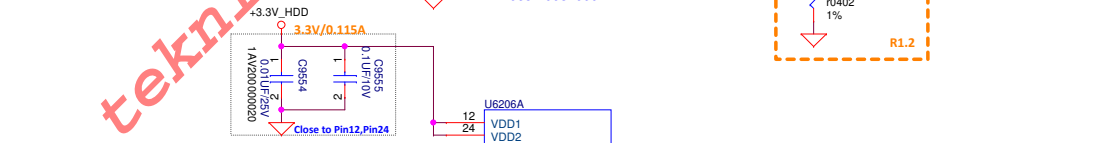
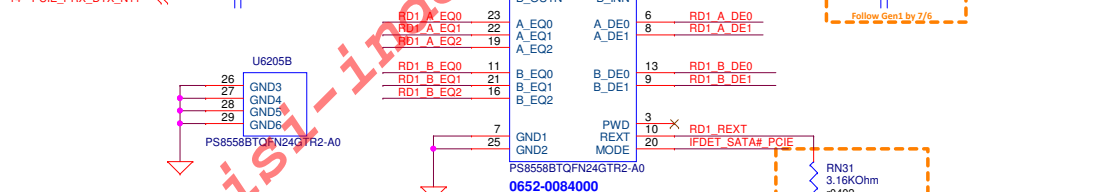
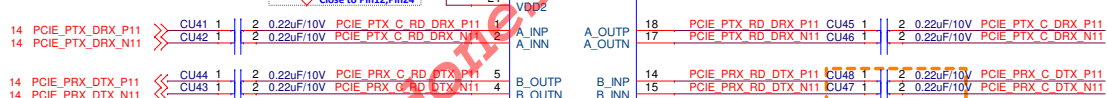
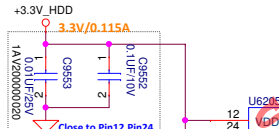
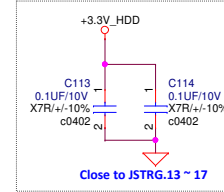
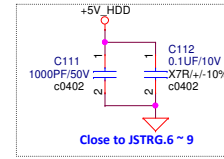
Programmable output de-emphasis level setting for channel B.
B_DE0: internally pulled up at ~150K
B_DE1 internally pulled down at ~150K
[B_DE1,B_DE0] ==

L/L -2 dB
H/L -7.5dB
L/H -3.5dB (default)
H/H -6 dB

IFDET_SATA#_PCIE	Device Interface
0 (default)	SATA
1	PCIE

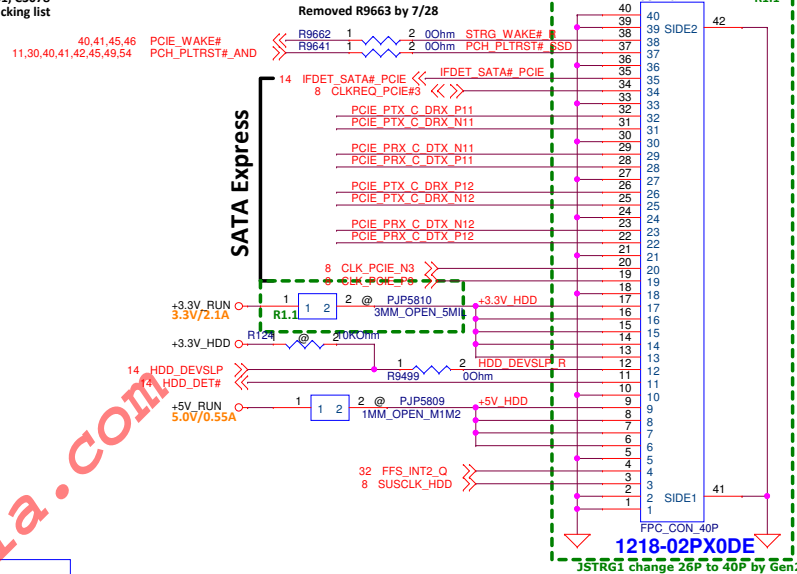
IFDET_SATA#_PCIE RC6171 2 100KOhm

Removed U34, R9565, R9566, C462, C9951, C3078
on +3.3V_HDD power control by 7/24 tracking list



CU31~CU36,CU49,CU50 change to 0.01uF from 0.22uF for SATA device by 7/31
CU31~CU36,CU49,CU50 change to 0.22uF from 0.01uF for SATA device by 8/7

Storage Connector



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TITLE	JSTRG1/PCIE_SATA Re-Driver
DWG NO.	CORE_B2
DATE	Friday, March 18, 2016
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REV.	2.0



P/N:DC010004C10

5V_HDD

FFS_INT2

3.3V_RUN

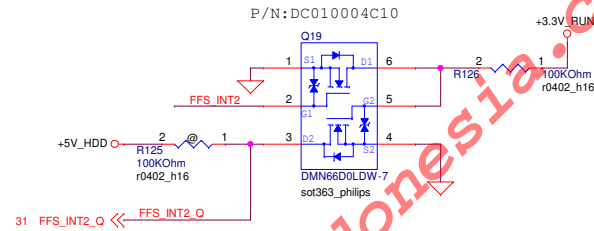
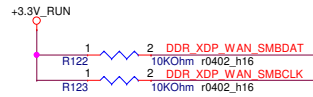
FFS_INT2_Q

R125 100KOhm r0402_h16

R126 100KOhm r0402_h16

DMN66D0LDW-7 sot363_philips

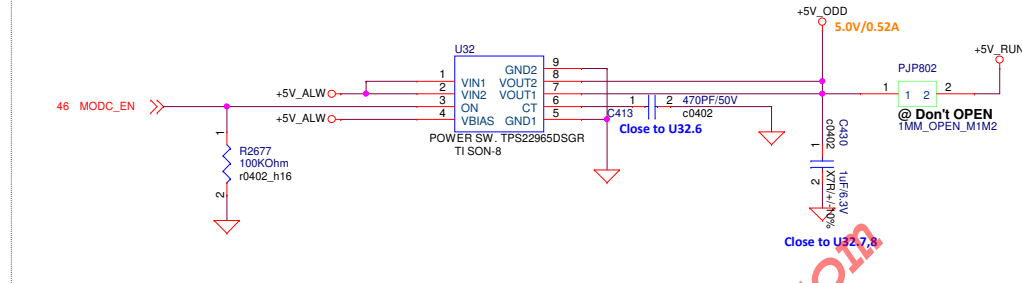
31 FFS_INT2_Q



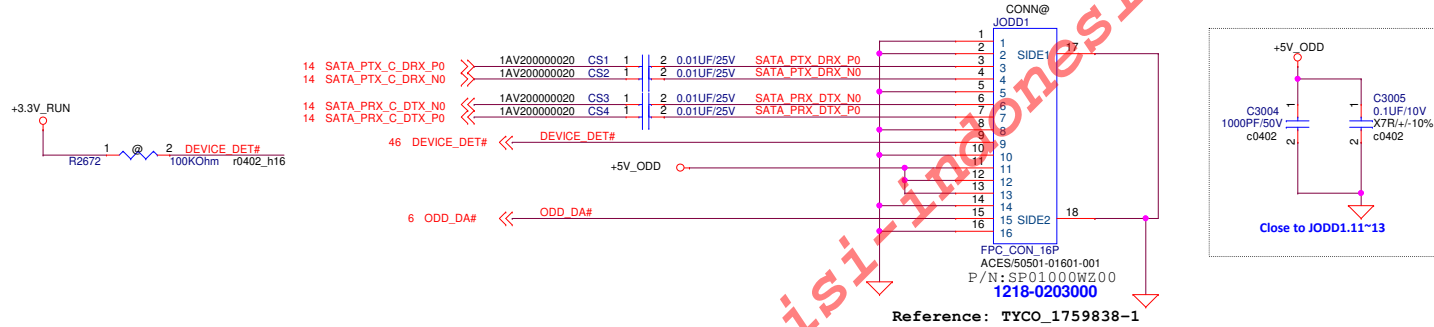
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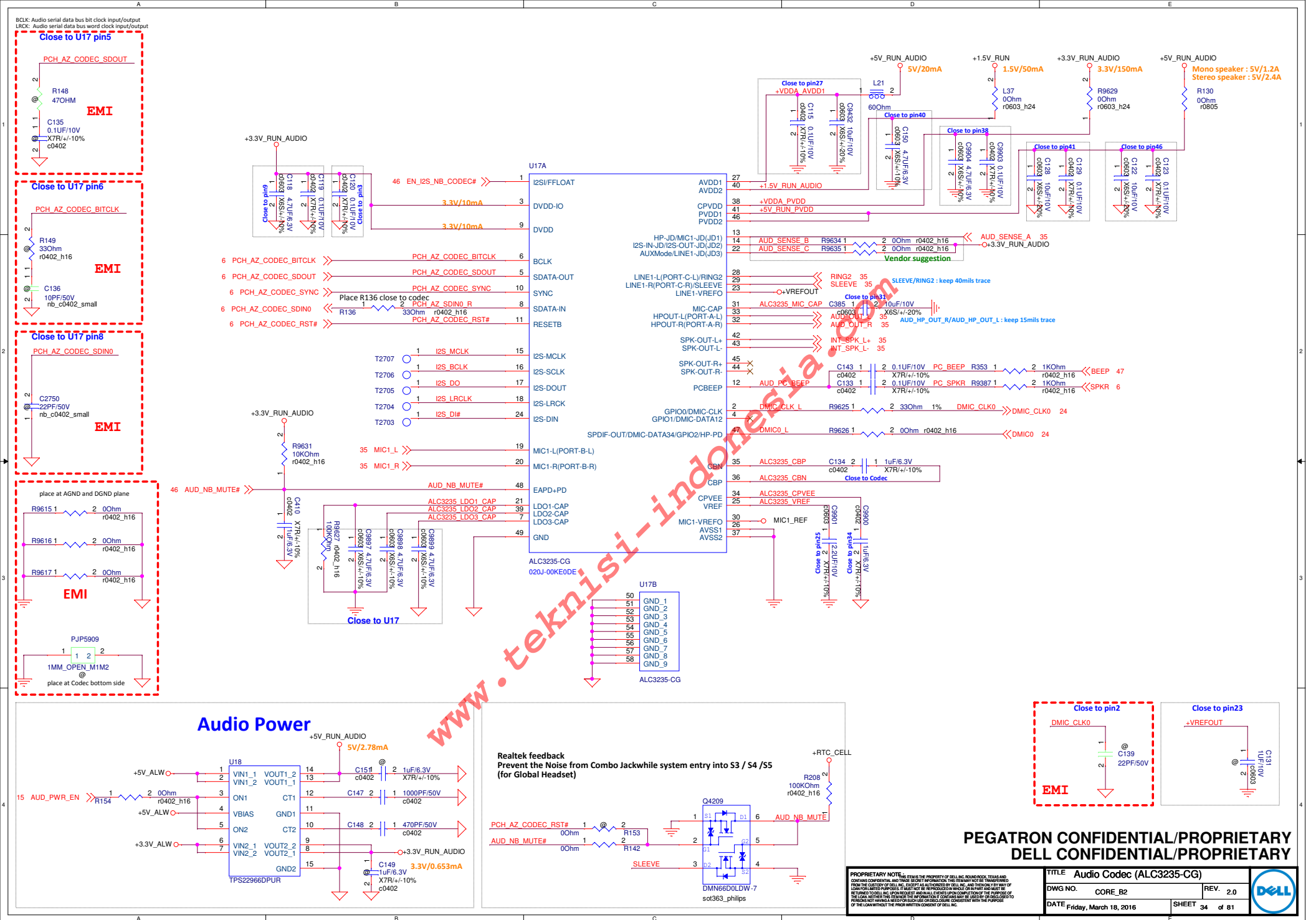


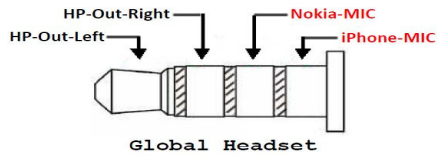
ODD power



ODD Connector



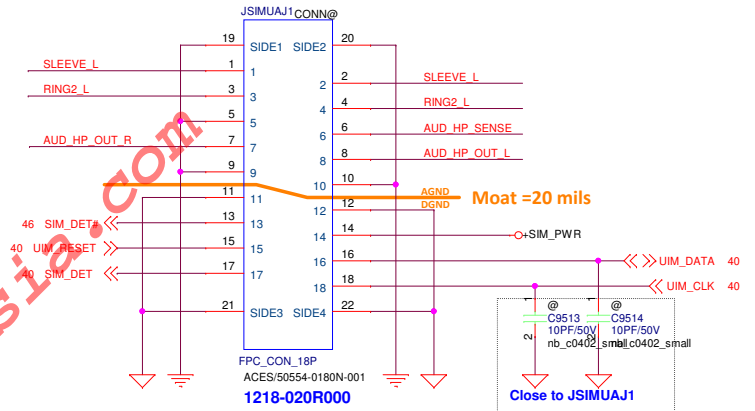
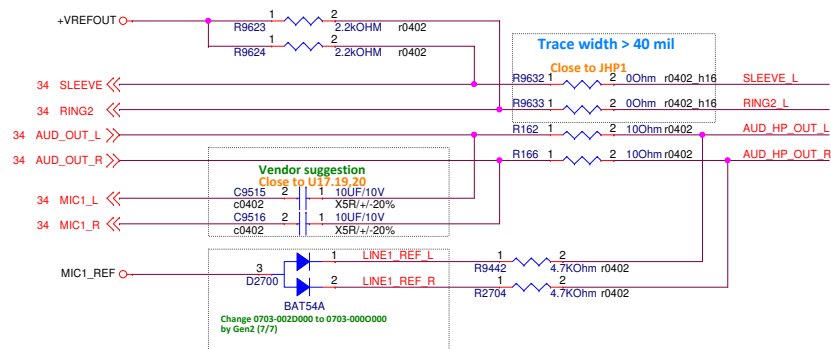
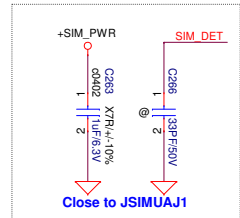




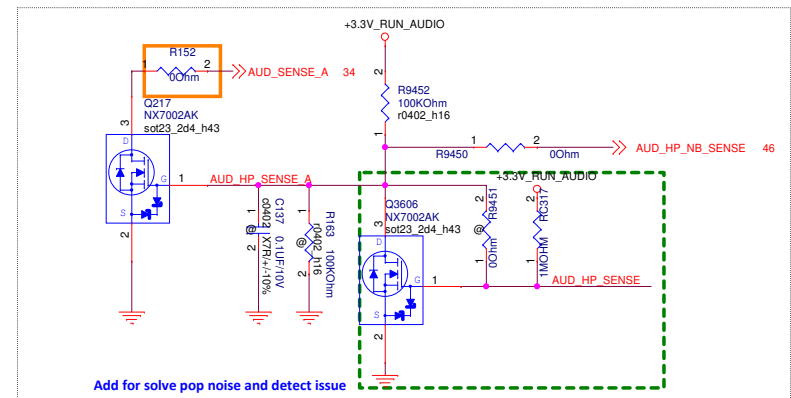
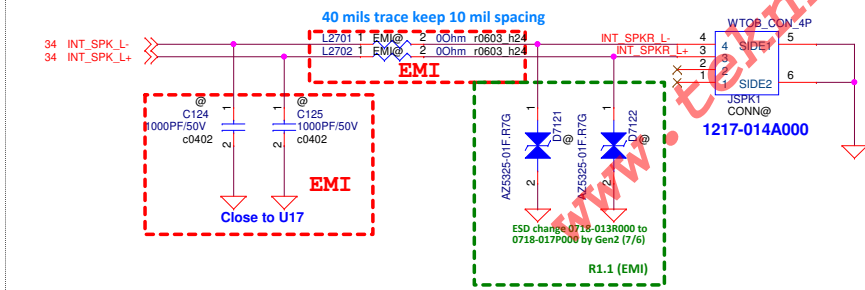
Dior Jack Requirements (Gen2):

1. Universal Audio jack (HP & mono mic).
2. Supports auto detect of both OMTP and CTIA headsets.
3. 3.5 mm jack with detect pin on tip.
4. Re-taskable to standard Microphone or Stereo Line Input.
5. Inline control support = Yes.
6. HP Amp power > 20 mW into 32ohm 1% THD+N.

uSIM + UAJ Connector



Internal Speaker Header (Mono)

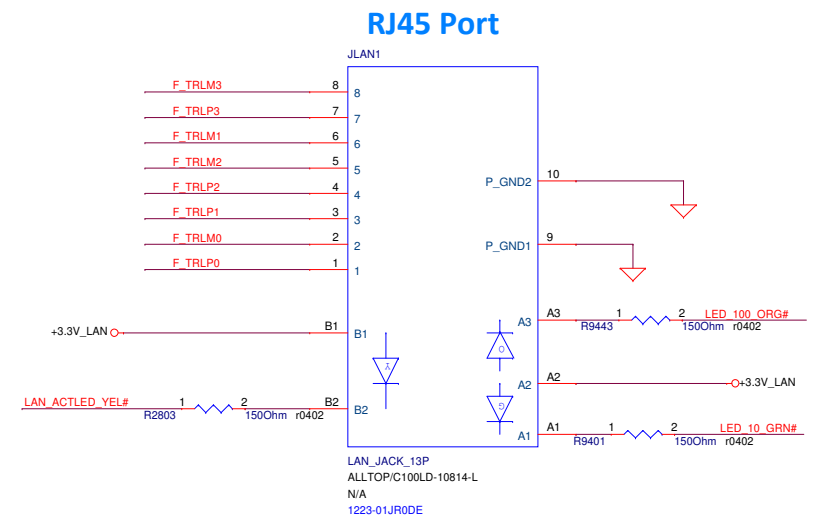
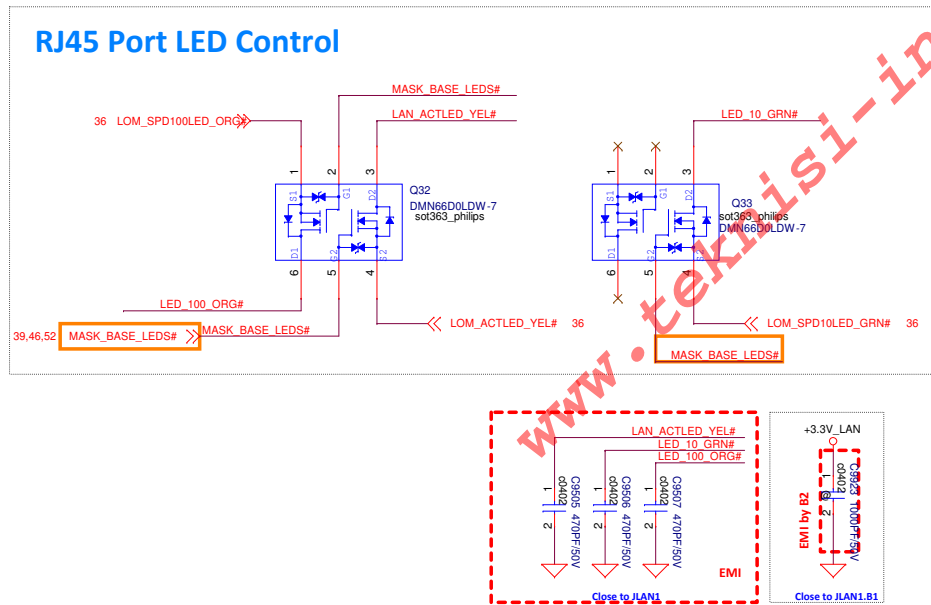
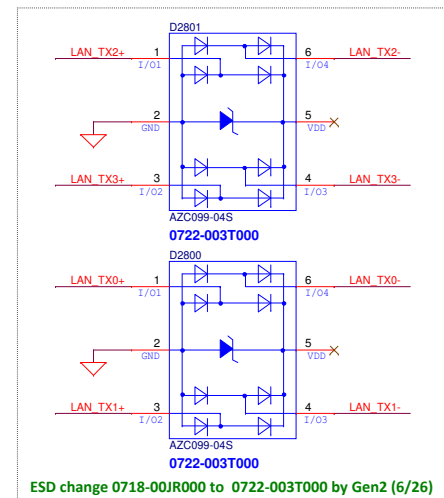
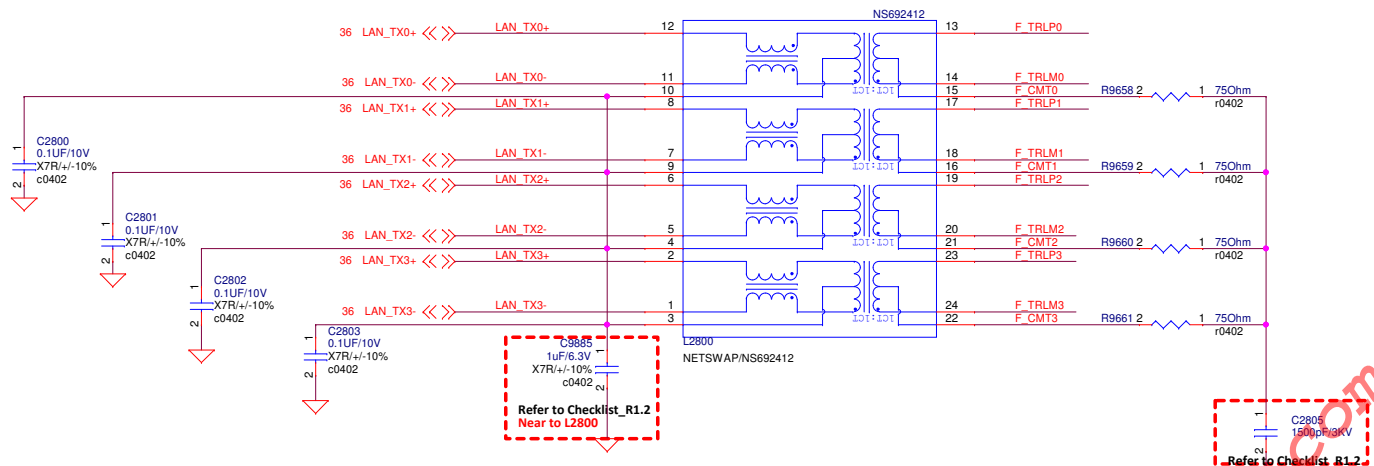


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TITLE	JSIMUAJ1/JSPK1
DWG NO.	CORE_B2
REV.	2.0
DATE	Friday, March 18, 2016
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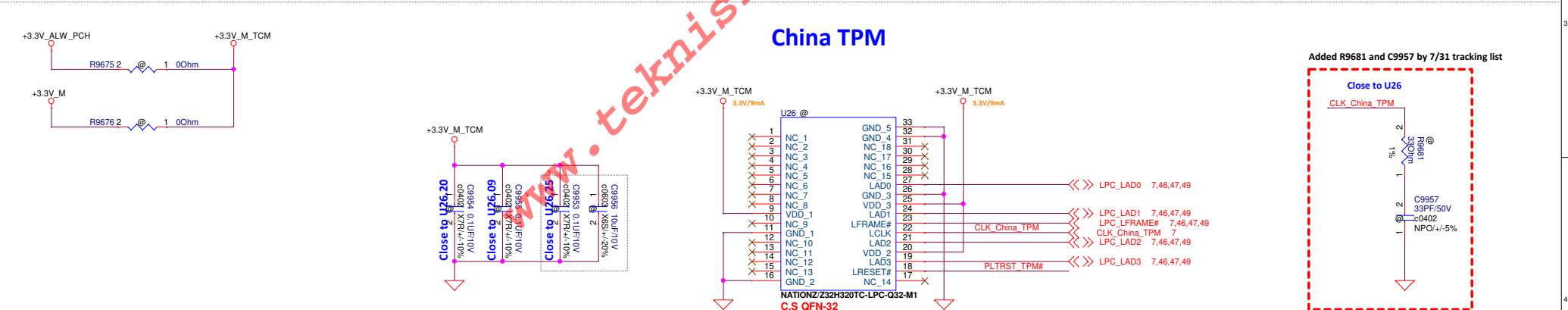
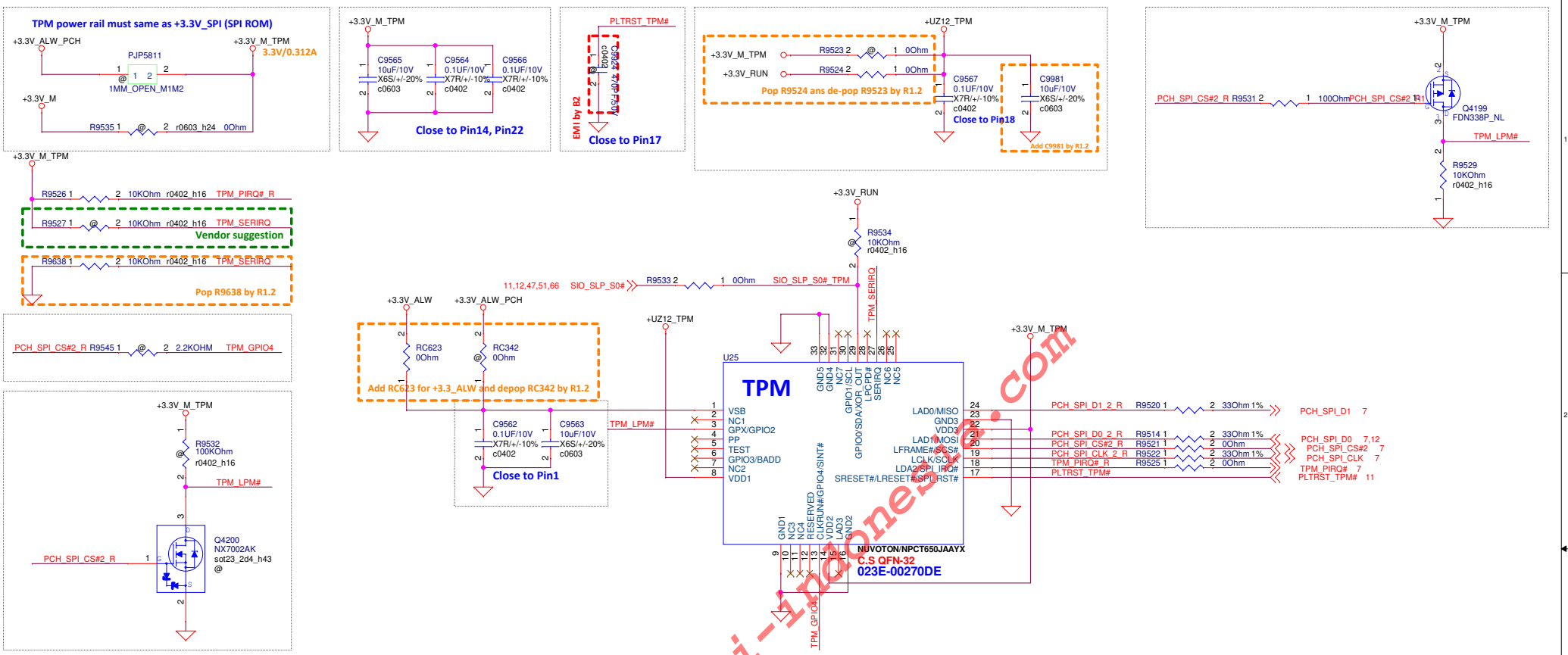




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DWG NO. CORE_B2		REV. 2.0	
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DWG NO.	CORE_B2	REV.	2.0
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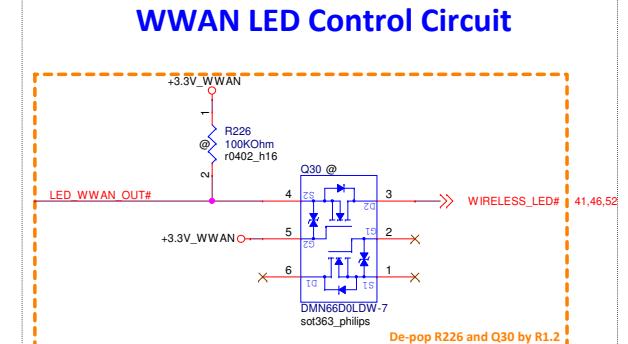
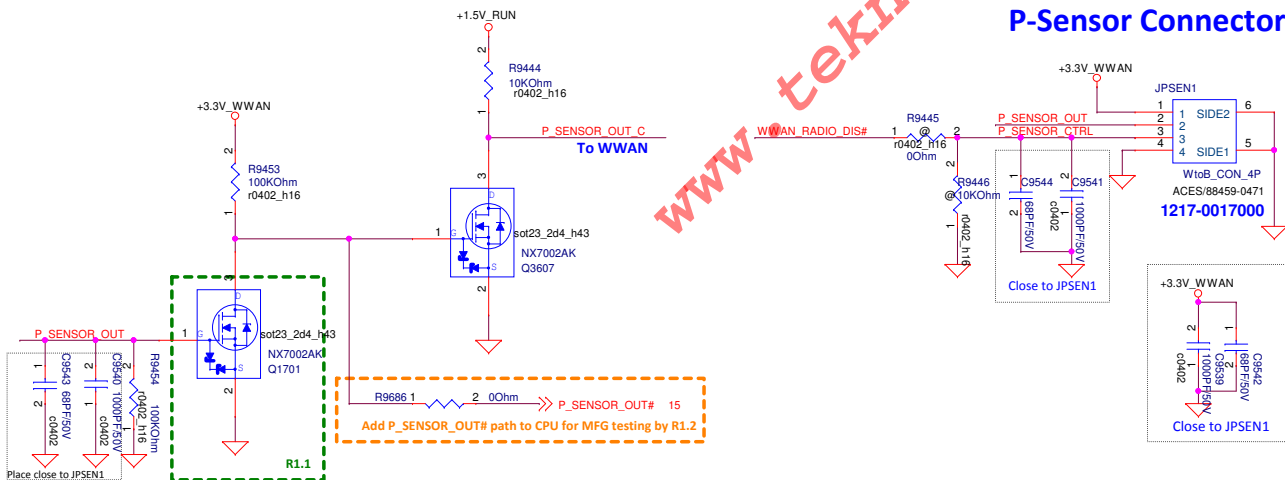
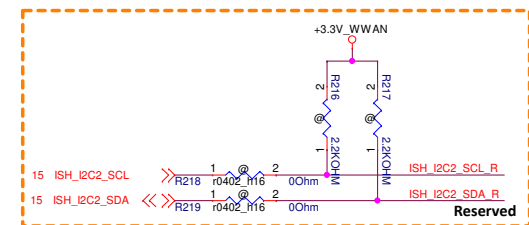
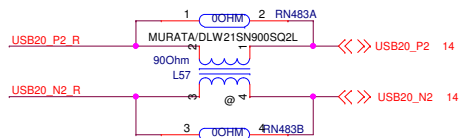
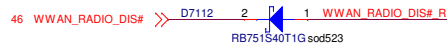
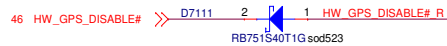
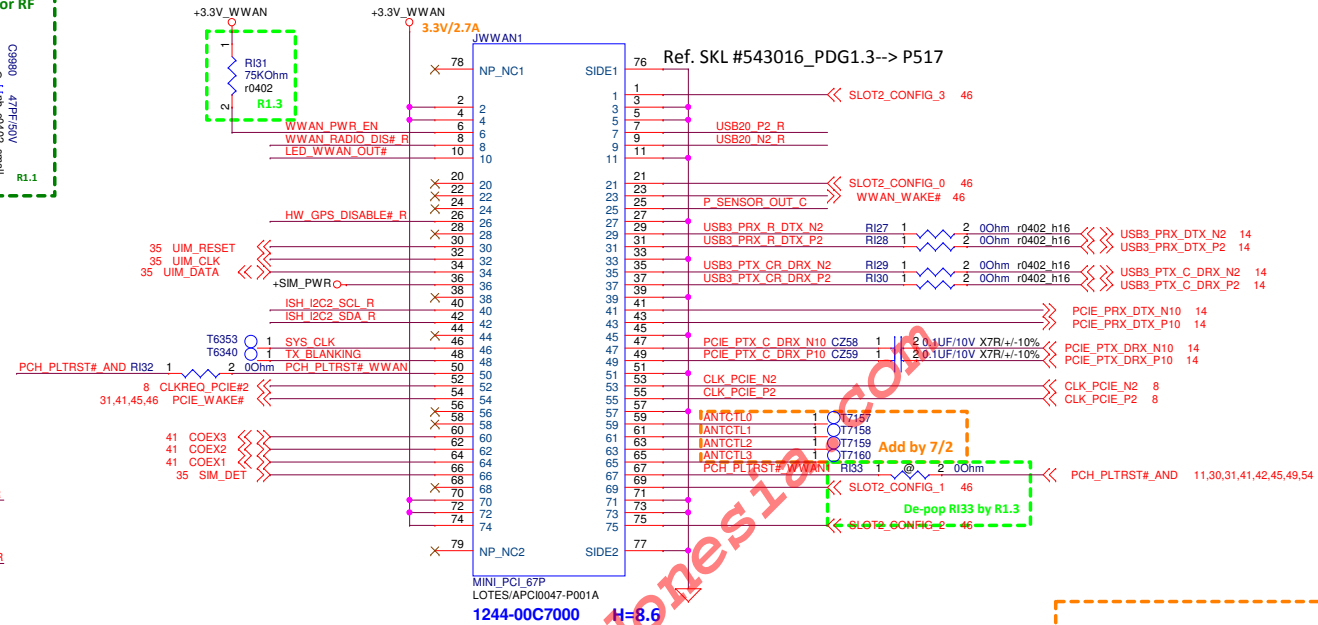
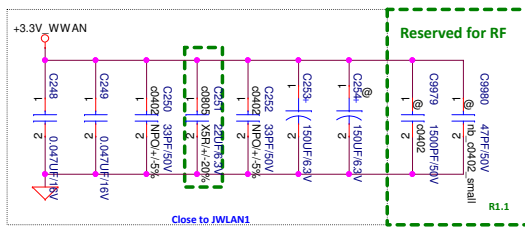
USB3 Hub

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TITLE		JIOR1/JSH1	
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NGFF KEY-B WWAN/LTE Connector



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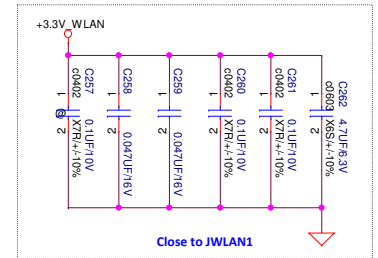
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TITLE	JWWAN1/JPSEN1
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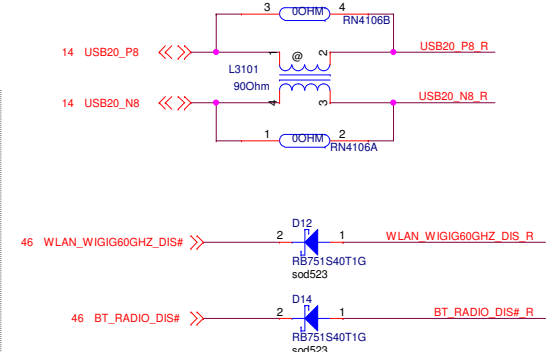
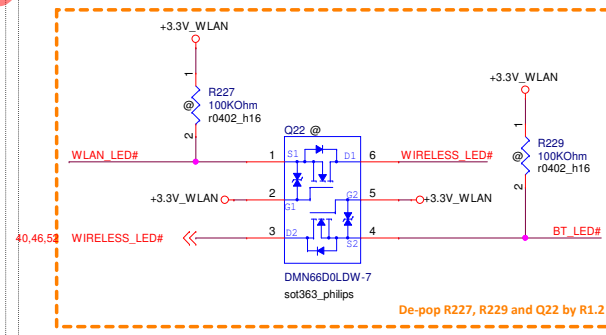
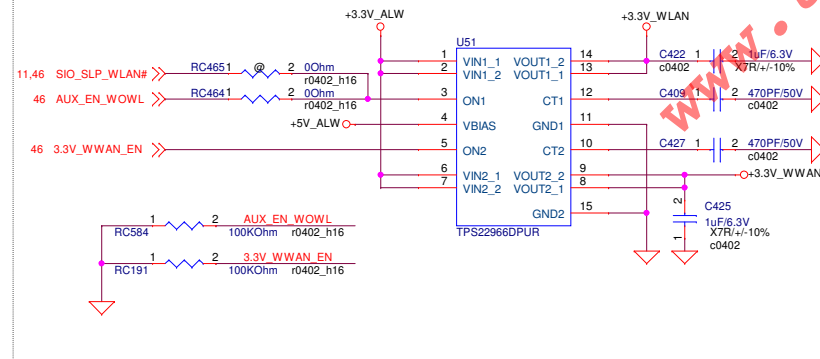
DWG NO.	CORE B2
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REV.	2.0
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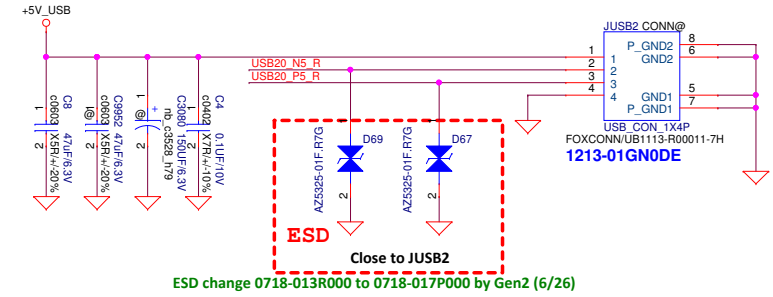
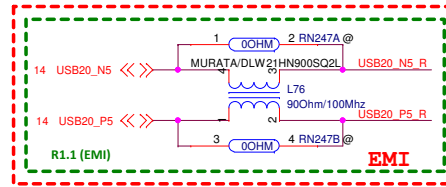
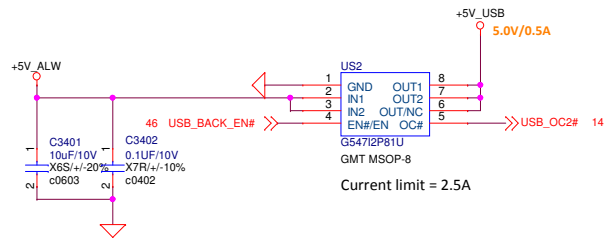


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 5 (Not wake enable)



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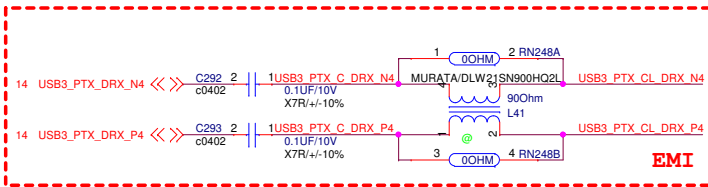
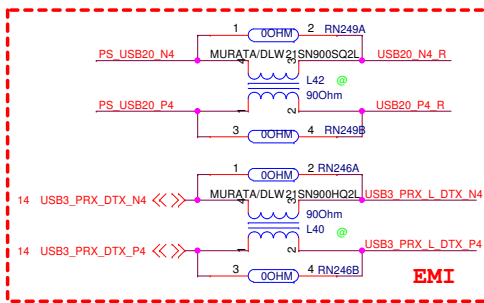
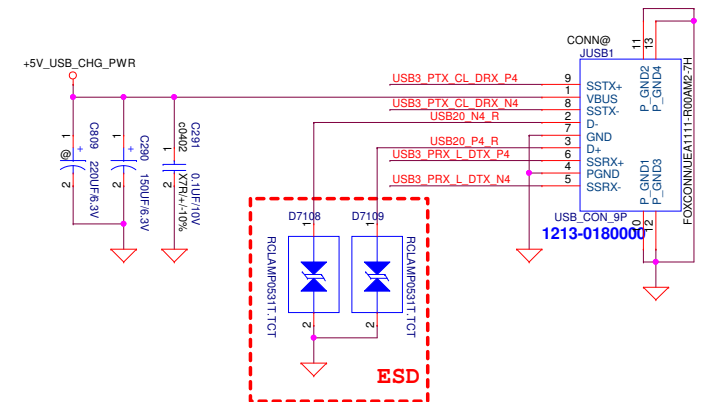
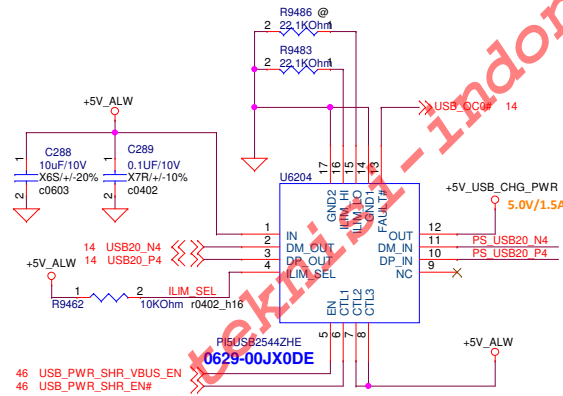
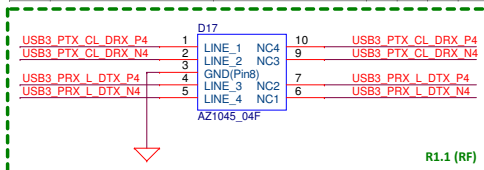




USB Charger

Ext USB Port (LEFT)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
ILIM_SEL Current Limit						
I_{OS}	OUT Current-limit ^(a)	$V_{BUS_SEL} = 0V, R_{ESEL_LO} = 210k\Omega$	205	240	275	
		$V_{BUS_SEL} = 0V, R_{ESEL_LO} = 400k\Omega$	275	325	380	
		$V_{BUS_SEL} = 0V, R_{ESEL_LO} = 221k\Omega$	3170	3750	4400	mA
t_{SP}	Response time to OUT short circuit ^(b)	$V_{BUS_SEL} = V_{BUS_RAMP}, R_{ESEL} = 20k\Omega$	2340	2510	2685	
		$V_{BUS_SEL} = V_{BUS_RAMP}, R_{ESEL} = 16.9k\Omega$	2770	2970	3170	
		$V_{BUS} = 5.0V, R = 0.1\Omega, \text{lead length} = 2"$	-	1.5	-	μs



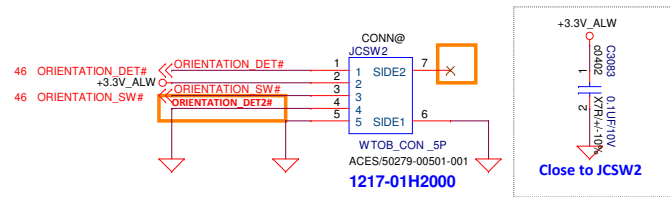
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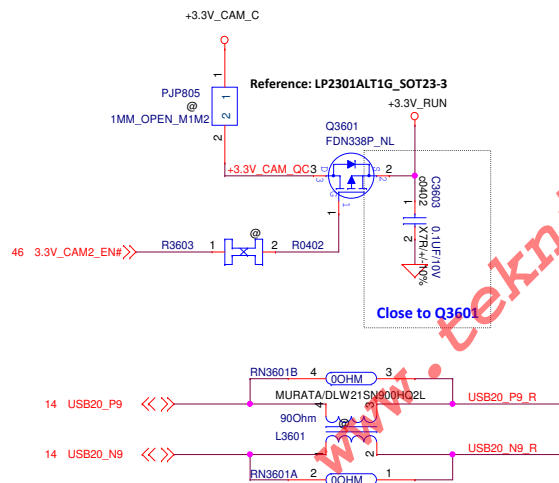
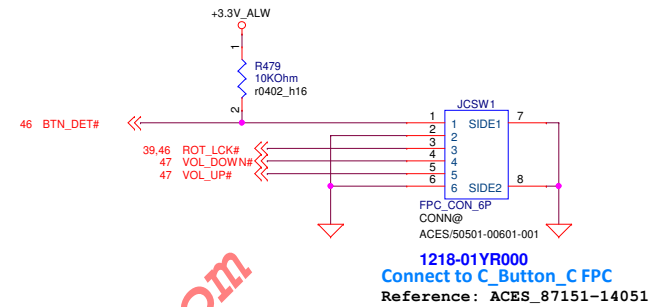
TITLE		JUSB1/JUSB2/USB Charger
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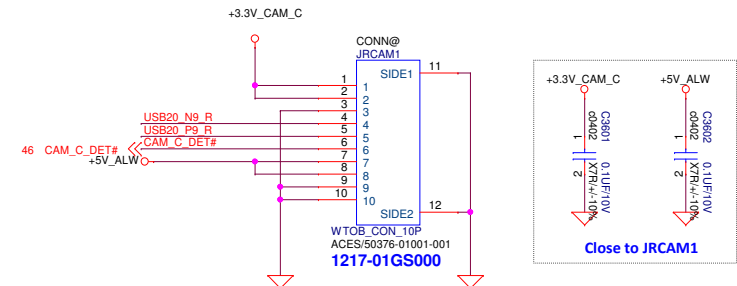
Columbus Hall Effect Connector



Columbus Button Connector



Columbus Rear Camera Connector

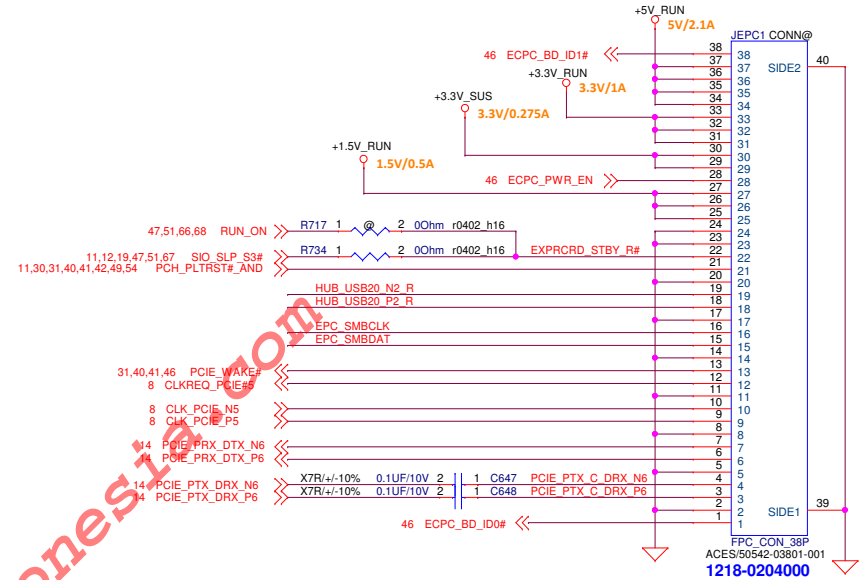
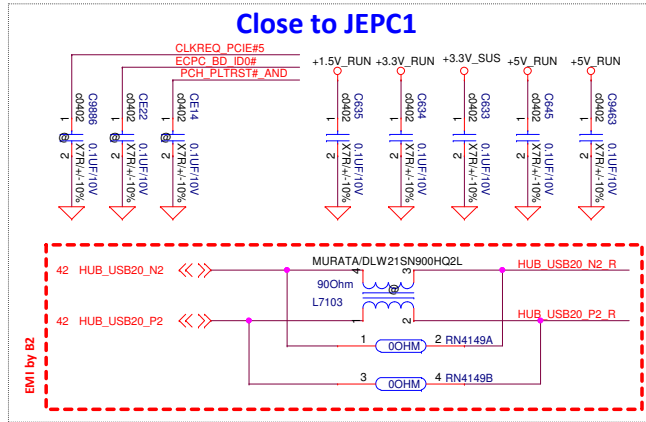
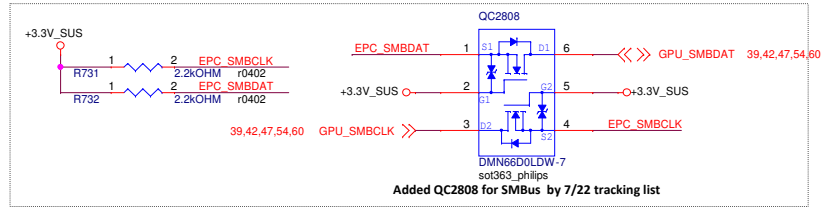


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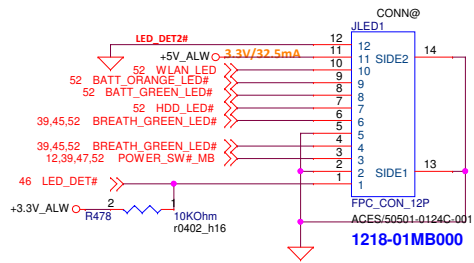
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TITLE JCSW1/JCSW2/JRCAM1		
DWG NO.	CORE_B2	
DATE	Friday, March 18, 2016	
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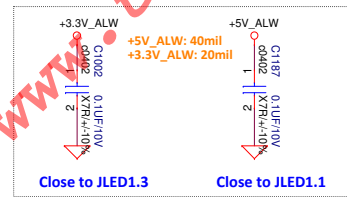
Express Card/PCMCIA Connector



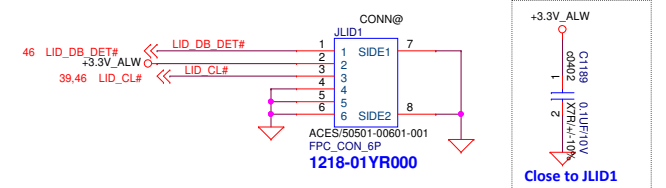
LED Connector



Connect to C_LED FPC

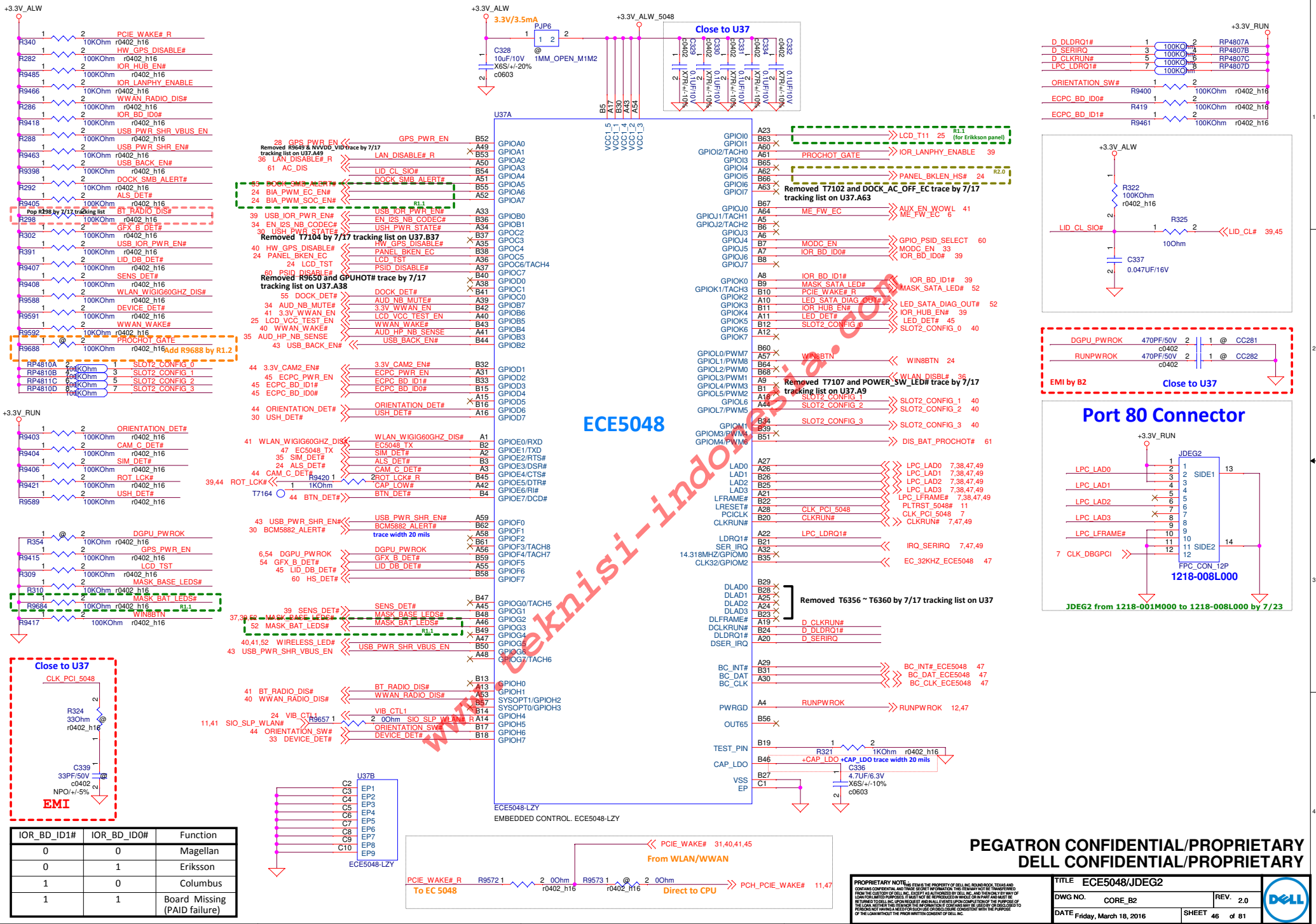


LID Connector

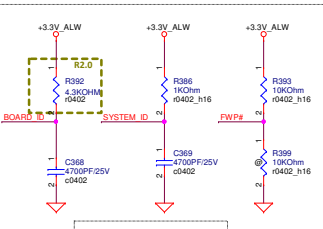
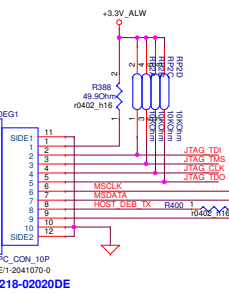
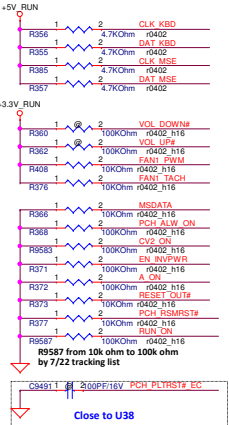
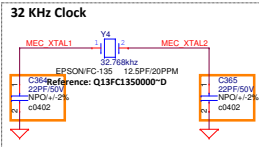


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DWG NO. CORE_B2	REV. 2.0		
DATE Friday, March 18, 2016	SHEET 45 of 81		

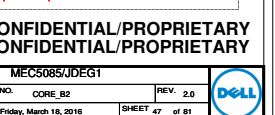
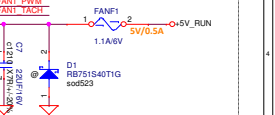
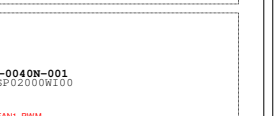
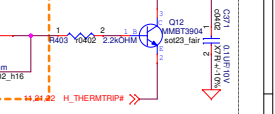
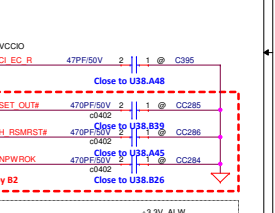
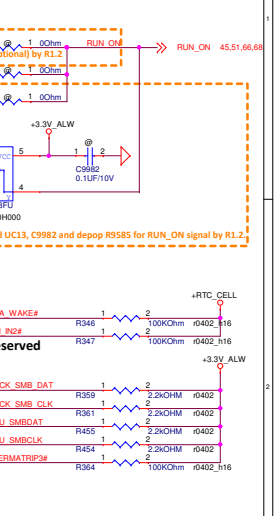
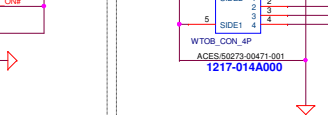
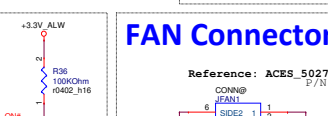
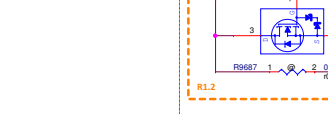
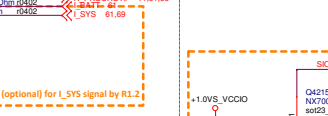
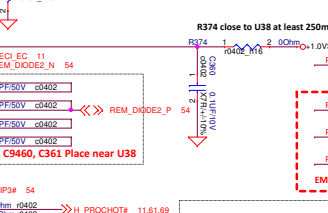
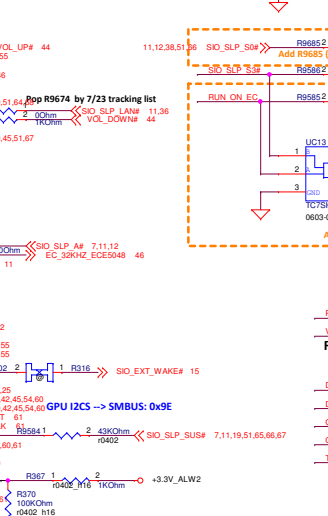
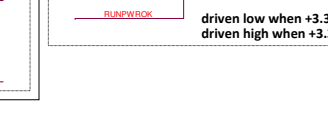
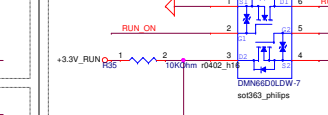
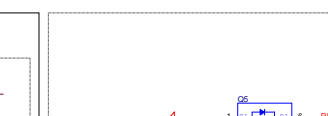
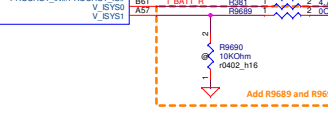
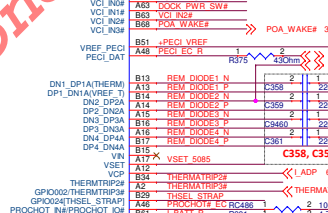
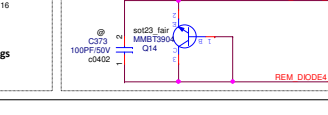
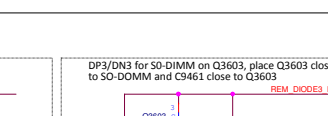
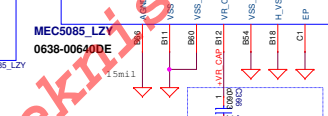
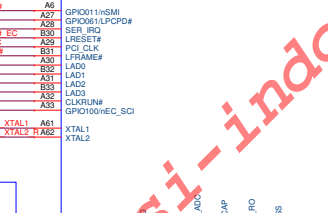
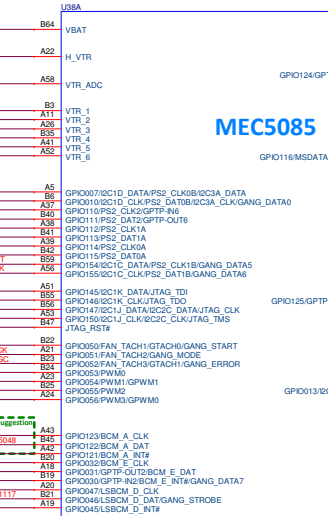
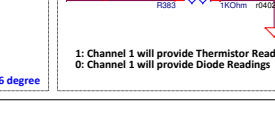
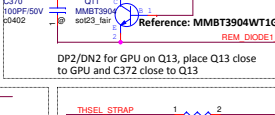
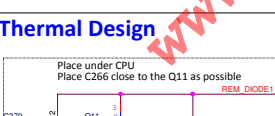
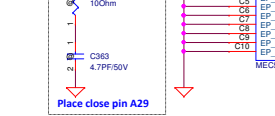
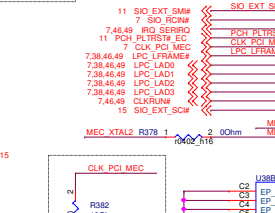
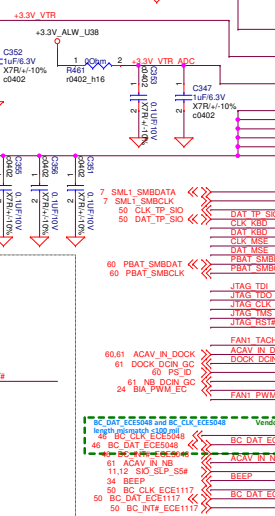
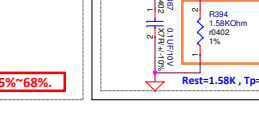
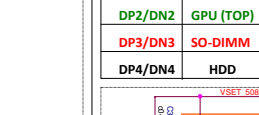
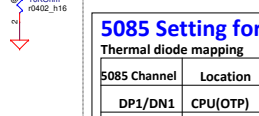
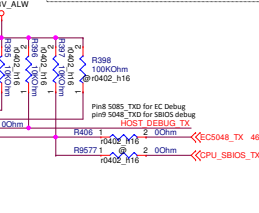
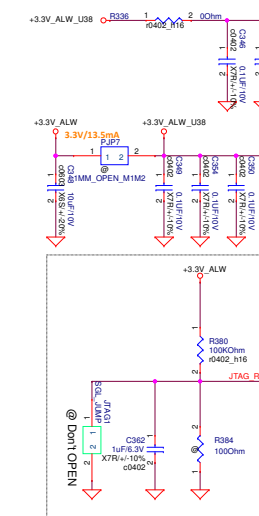


IOR_BD_ID#	IOR_BD_ID#	Function
0	0	Magellan
0	1	Eriksson
1	0	Columbus
1	1	Board Missing (PAID failure)



CHIPSET_ID for BID function
R392 240K
C368 4700pF/25V
REV X00
130K 4700p X01
62K 4700p X02
33K 4700p X03
8.2K 4700p X04
4.3K 4700p A00
2K 4700p A01
1K 4700p A02
A03

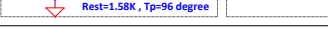
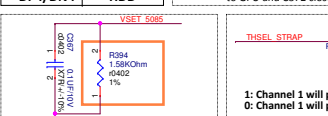
BOARD_ID rise time is measured from 5%~68%.



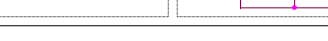
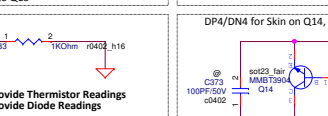
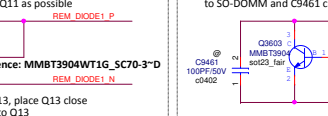
5085 Setting for Thermal Design

Thermal diode mapping

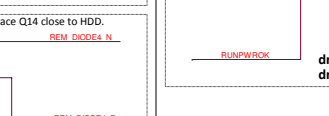
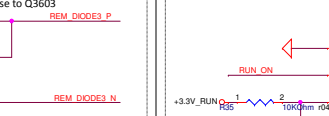
5085 Channel	Location
DP1/DN1	CPU(OTP)
DP2/DN2	GPU (TOP)
DP3/DN3	SO-DIMM
DP4/DN4	HDD



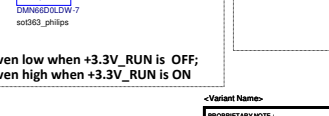
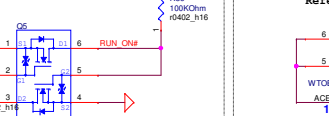
Place under CPU
Place C266 close to the Q11 as possible



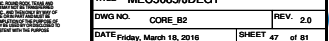
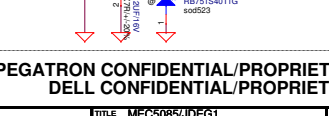
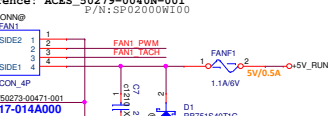
DP3/DN3 for SO-DIMM on Q3603, place Q3603 close to SO-DIMM and C9461 close to Q3603



DP2/DN2 for GPU on Q13, place Q13 close to GPU and C372 close to Q13

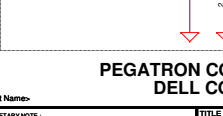
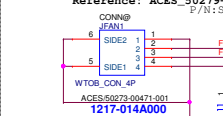


DP4/DN4 for Skin on Q14, place Q14 close to HDD.

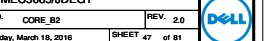
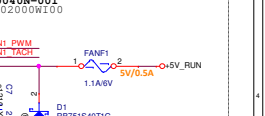


FAN Connector

Reference: ACES_50279-0040N-001
P/N:SP02000W100



driven low when +3.3V_RUN is OFF;
driven high when +3.3V_RUN is ON




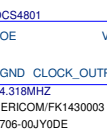
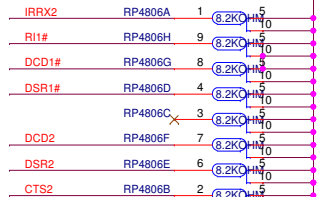
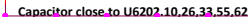
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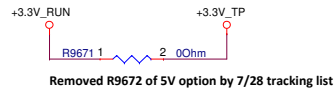




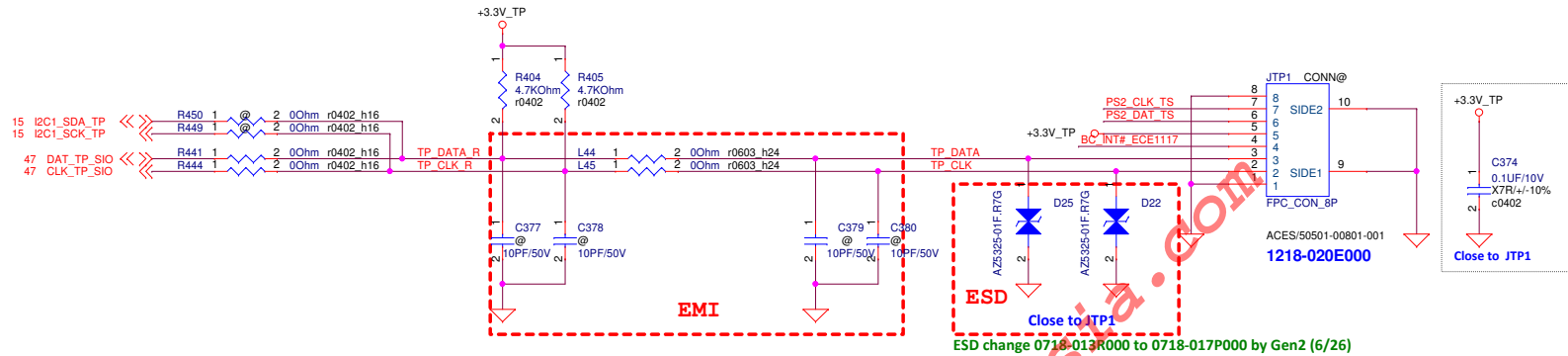
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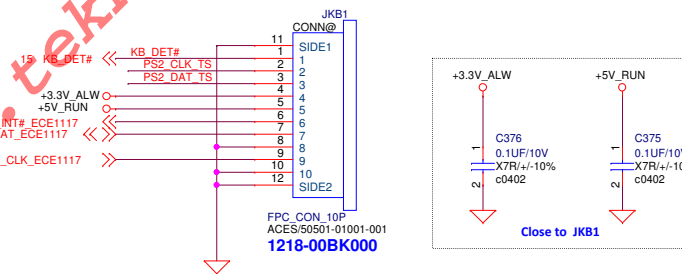
Touch Pad Power



Touch Pad Connector



KB Module Connector



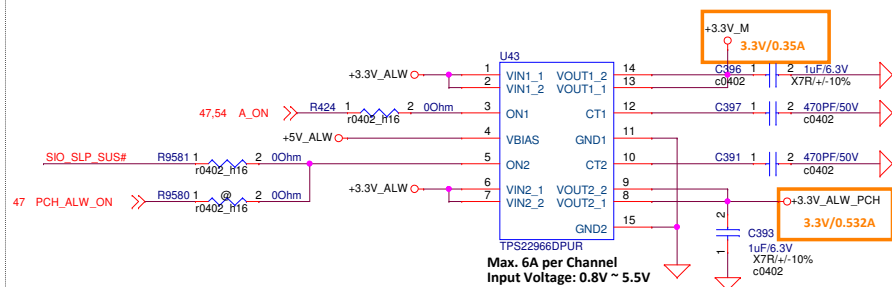
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DWG NO. CORE_B2		REV. 2.0	
DATE Friday, March 18, 2016		SHEET 50 of 81	

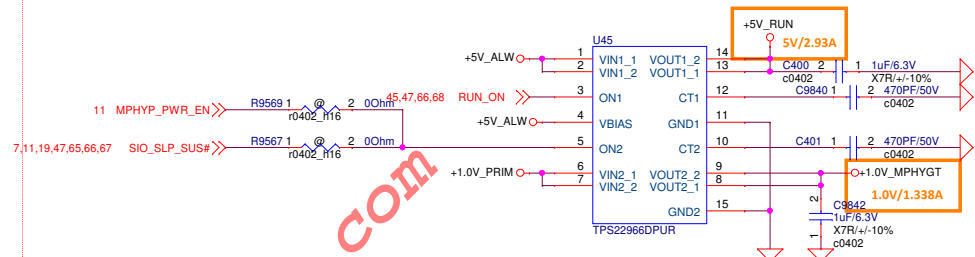


DC/DC Interface

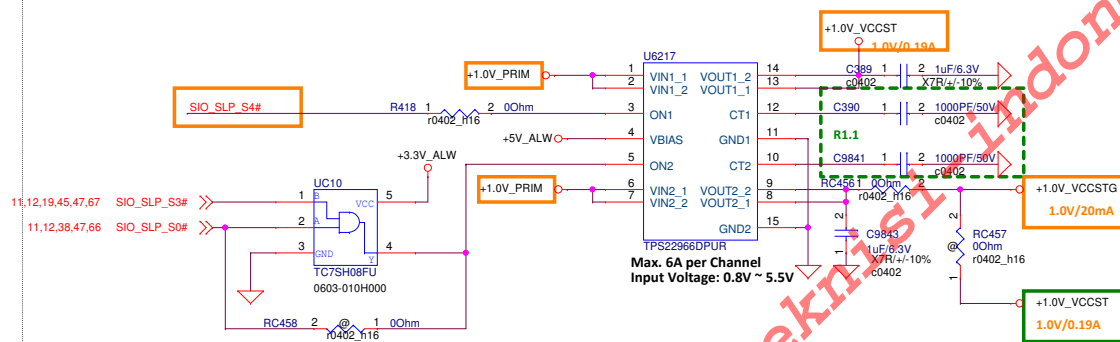
+3.3V_M / +3.3V_ALW_PCH Source



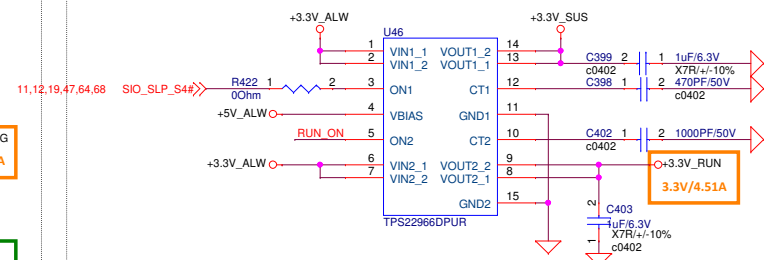
+5V_RUN / +1.0V_MPHYGT Source



+1.0V_VCCST / +1.0V_VCCSTG Source



+3.3V_RUN/+3.3V_SUS Source



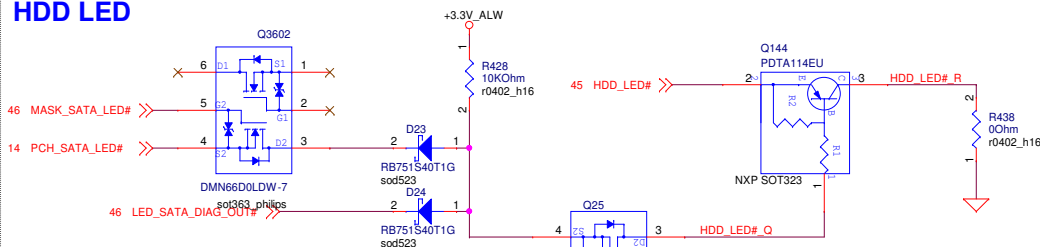
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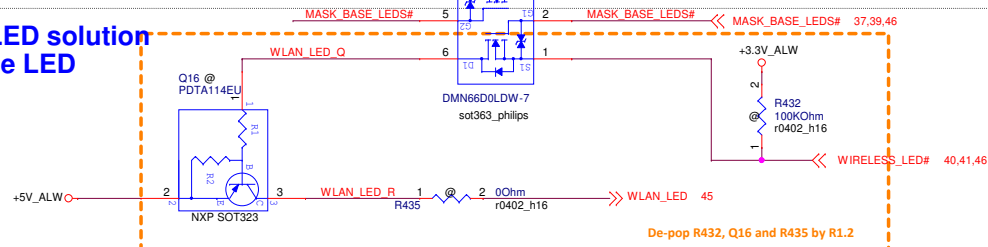
TITLE		Load Switch	
DWG NO.		CORE_B2	REV. 2.0
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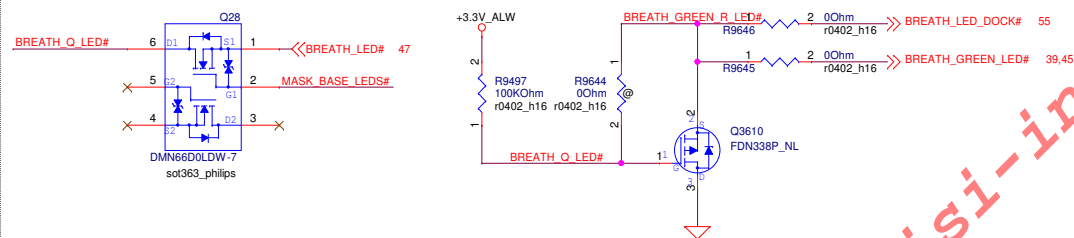
HDD LED



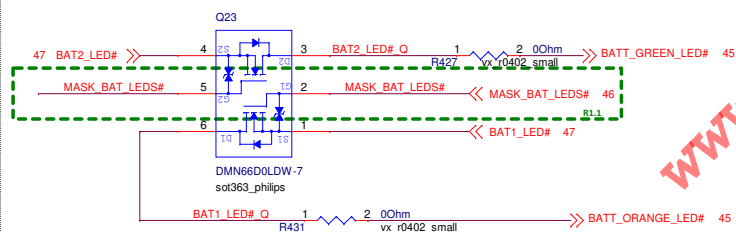
WLAN LED solution for White LED



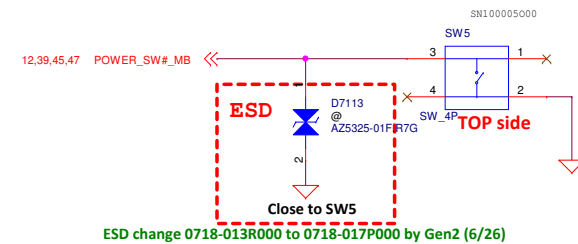
Breath LED



Battery LED



POWER SWITCH



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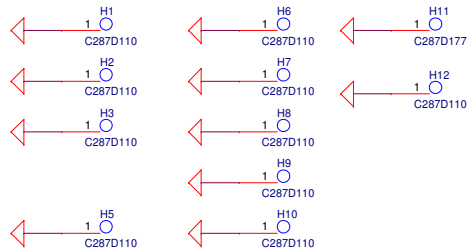
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TITLE LED Control Circuit		
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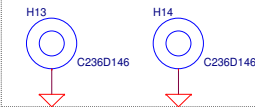
Screw Hole

Screw Hole $\Phi 2.8\text{mm}$ X7.3

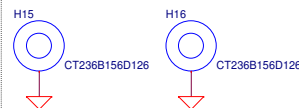


STANDOFF

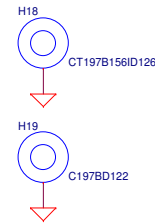
WWAN/WLAN STANDOFF



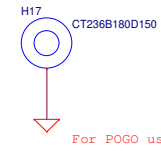
EDP STANDOFF



GPU STANDOFF

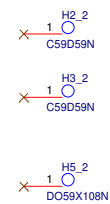


PEM STANDOFF

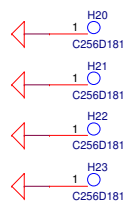


Tooling Hole

Tooling Hole



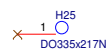
Tooling Hole



NPTH hole



NPTH hole



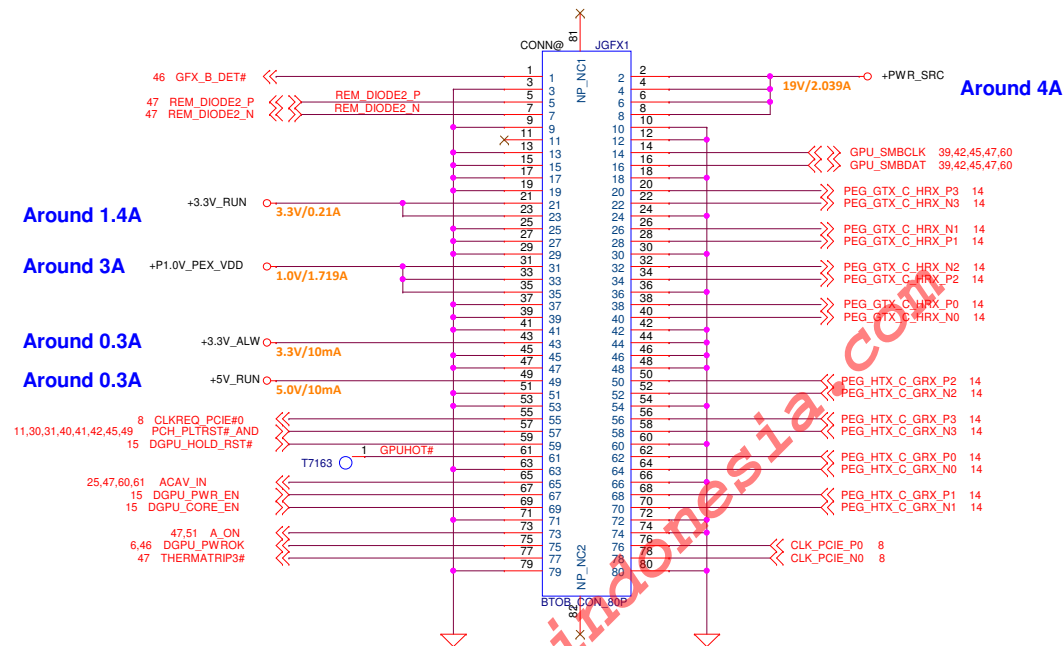
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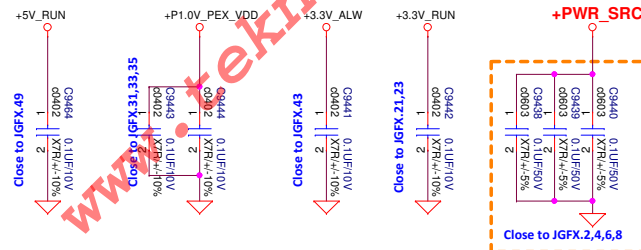
TITLE Mechanical Hole/Standoff		
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SAMTEC/LSHM-140-06.0-F-DV-A-N
1216-016G0DE

- For GFX conn power:
1. +PWR_SRC : 3.3A
 2. +P1.05V_PEX_VDD: 1.15A
 3. +3.3V_RUN: 0.342A
 4. +3.3V_ALW: 0.04A

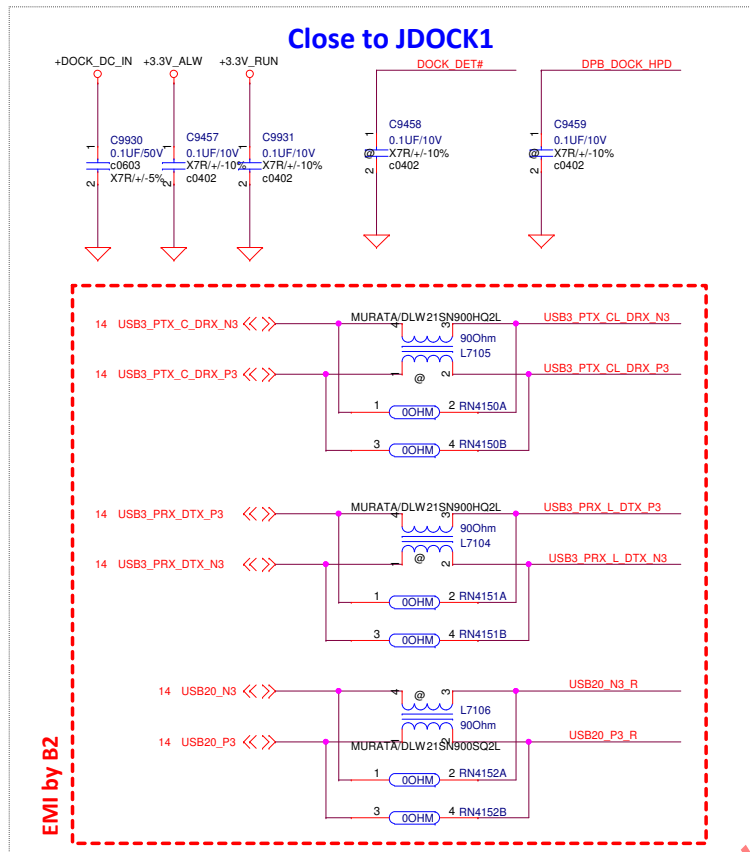


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TITLE JGFX1		
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Docking Connector

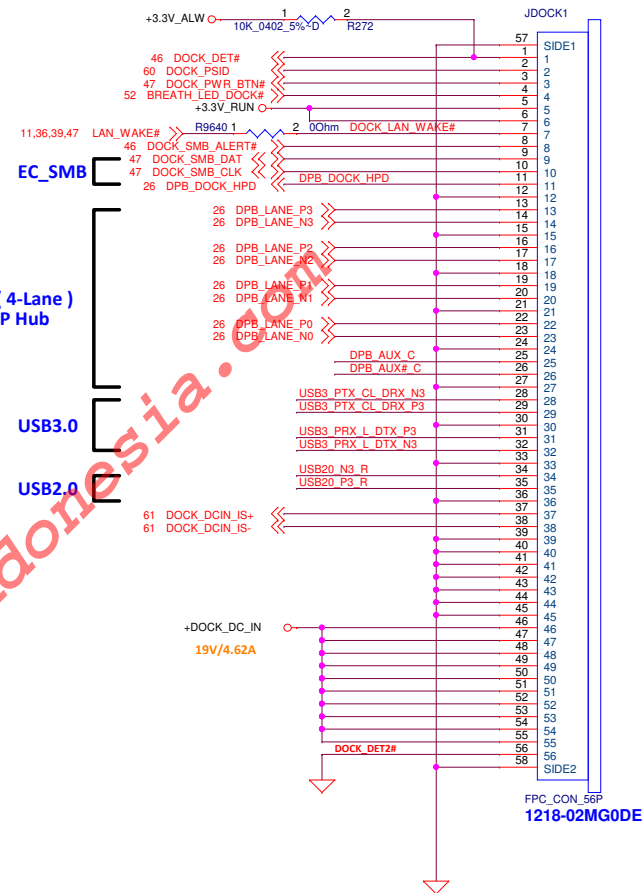


26 DPB_AUX# X7R/+/-10% 0.1UF/10V 2 1 C9948 DPB_AUX# C
26 DPB_AUX# X7R/+/-10% 0.1UF/10V 2 1 C9949 DPB_AUX# C


DP1.2 (4-Lane)
from DP Hub

USB3.0

USB2.0



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DWG NO. CORE_B2		REV. 2.0	
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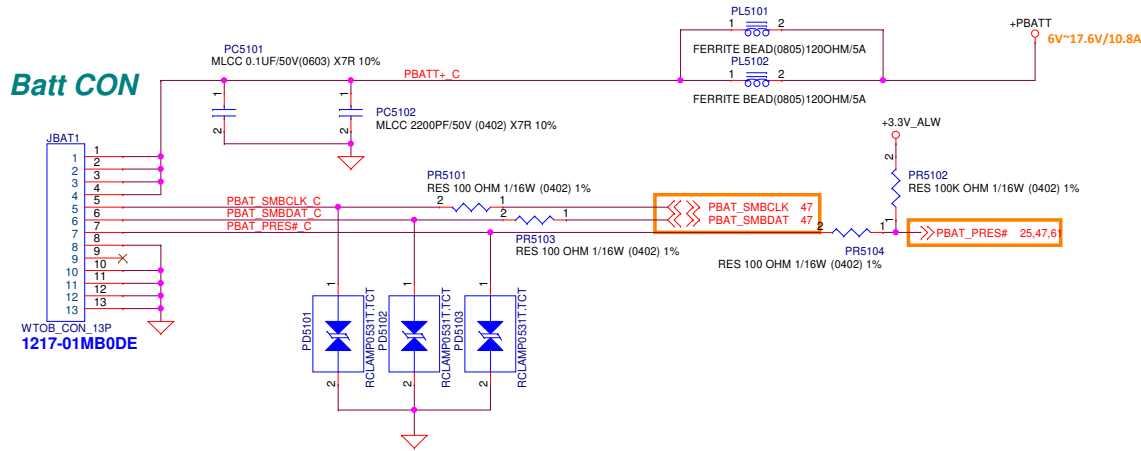
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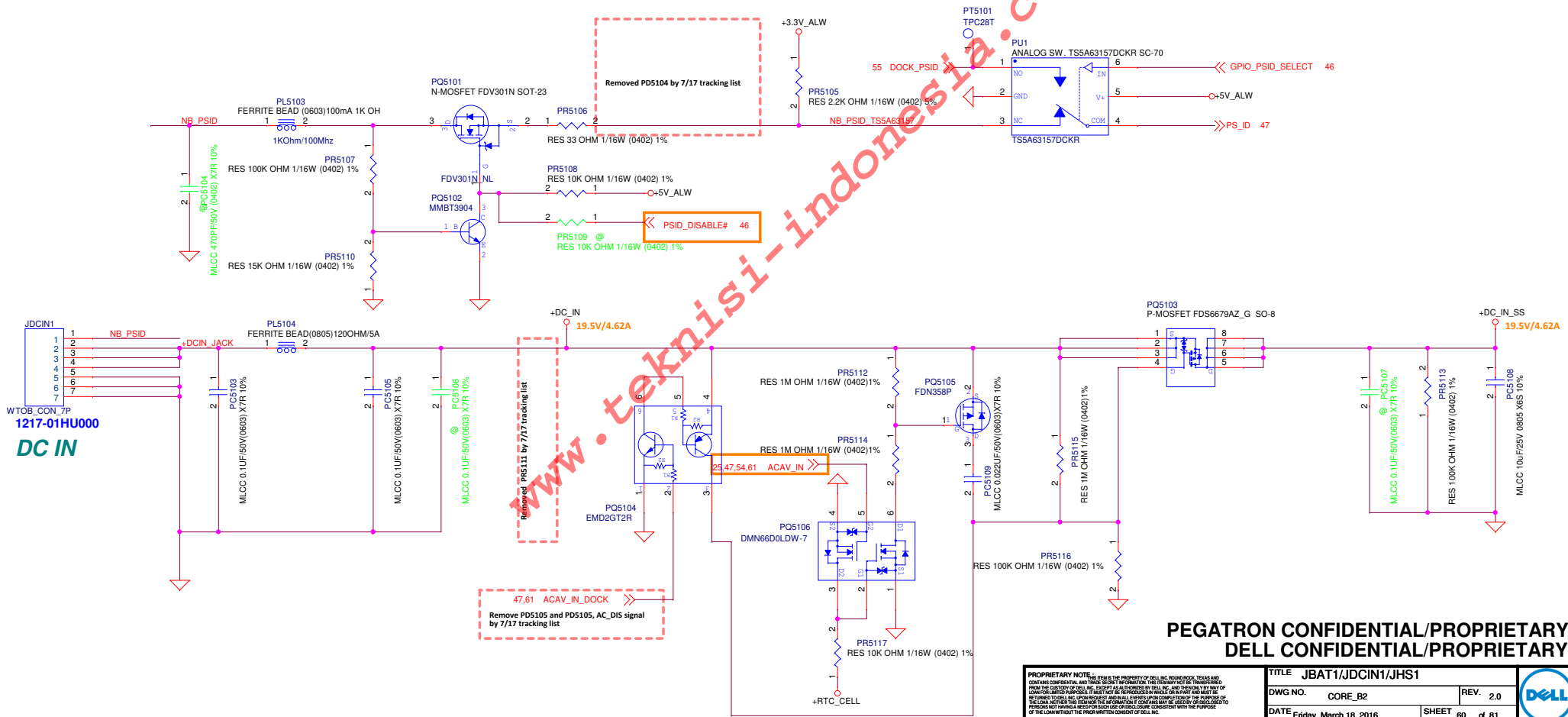
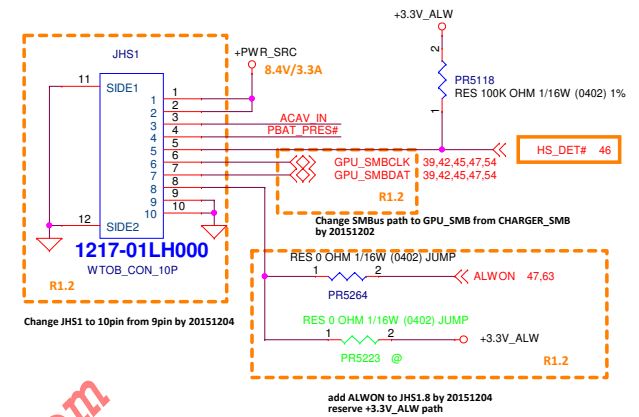
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Batt CON




Hot Swap Conn.



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TITLE		JBAT1/JDCIN1/JHS1		
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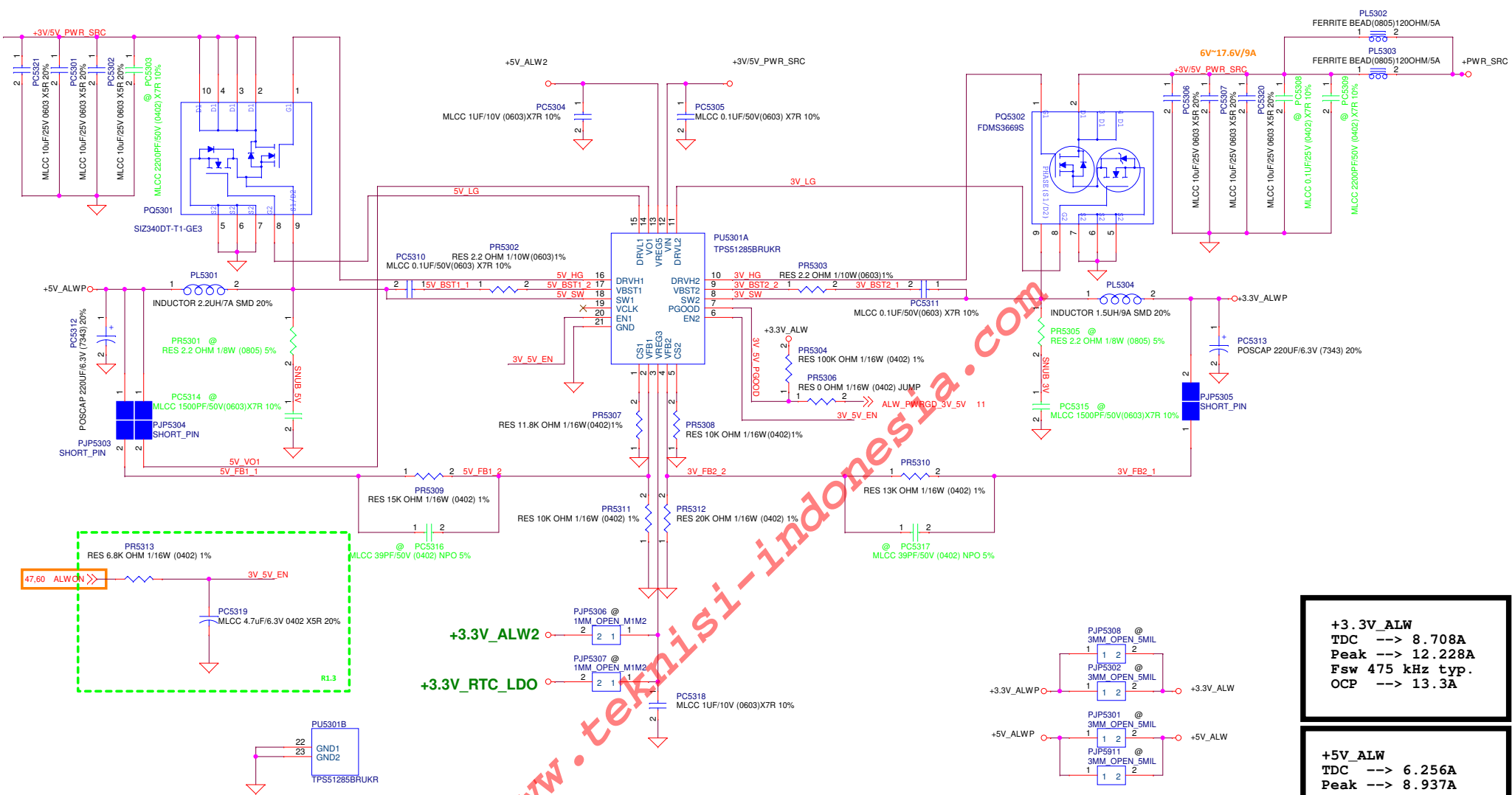
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+3.3V_ALW
TDC --> 8.708A
Peak --> 12.228A
Fsw 475 kHz typ.
OCP --> 13.3A

+5V_ALW
TDC --> 6.256A
Peak --> 8.937A
Fsw 400 kHz typ.
OCP --> 11.5A

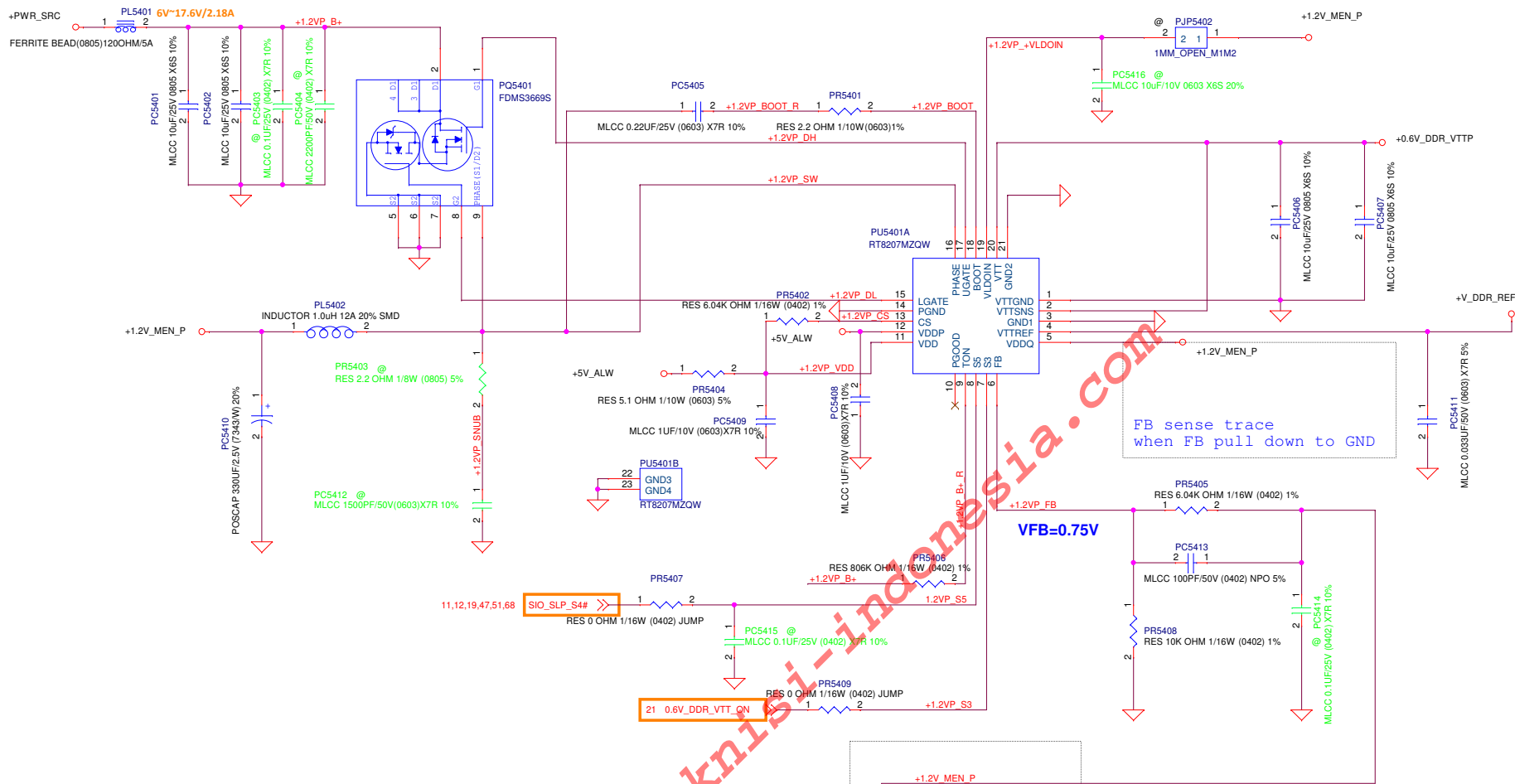
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+0.6V_DDR_VTT
TDC --> 1.05A
Peak --> 1.5A

+1.2V_MEM
TDC --> 8.75A
Peak --> 12.25A
OCP --> 14A
Fsw=300 kHz

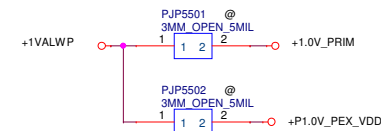
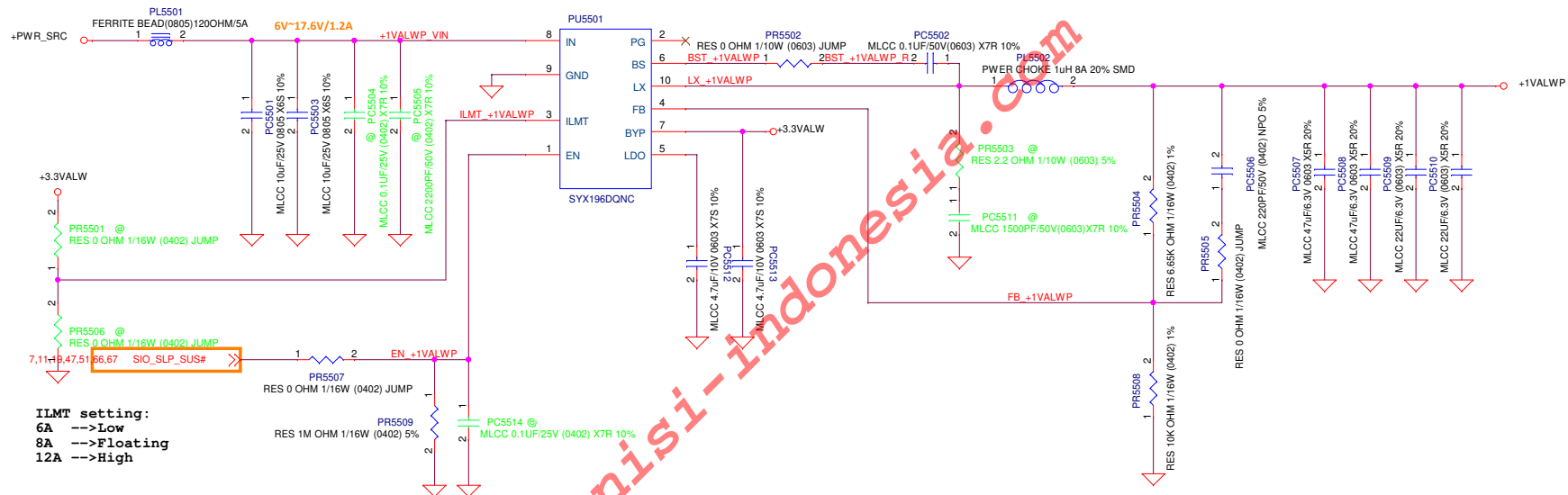
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TITLE +0.6V_DDR_VTT/+1.2V_MEM

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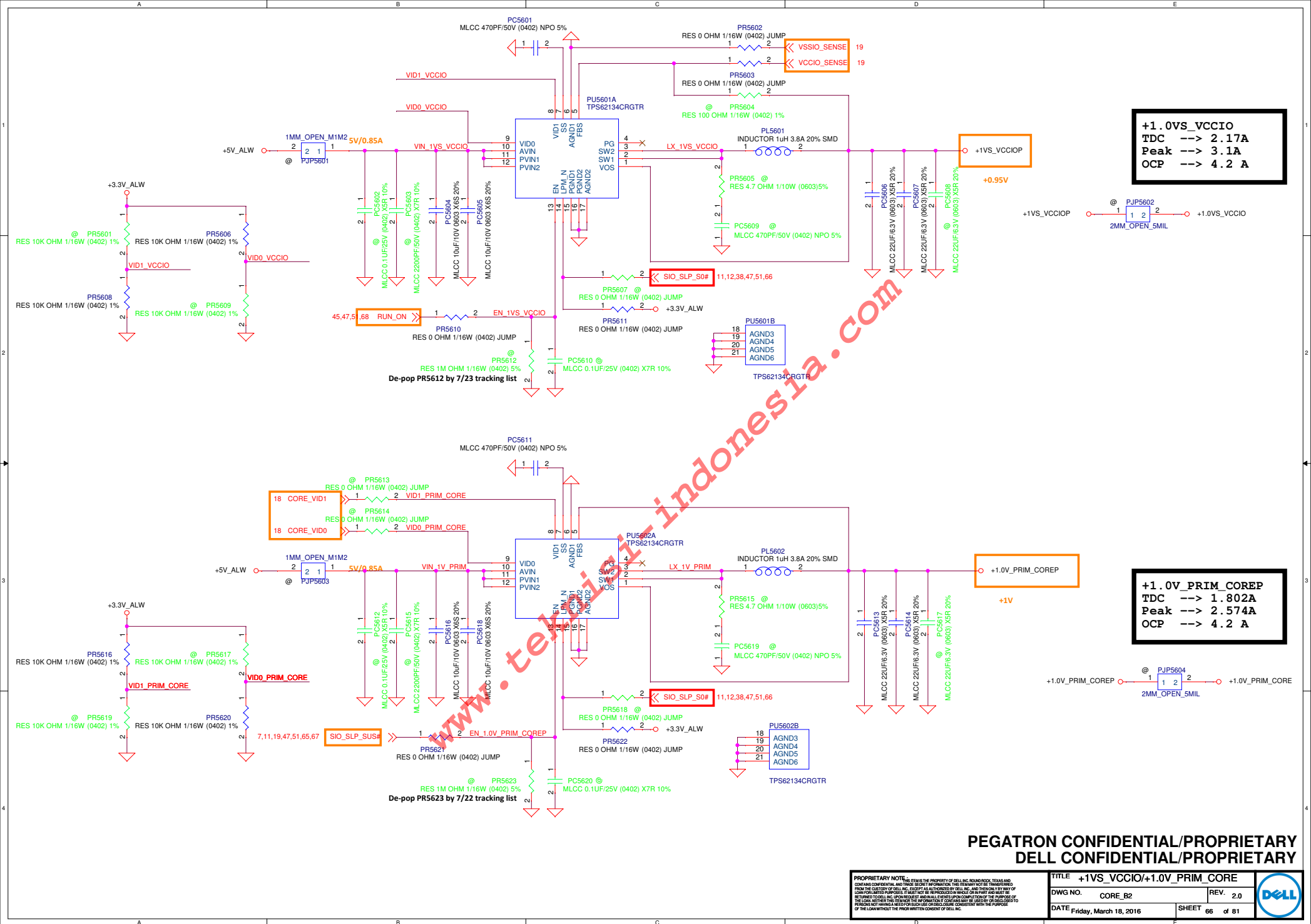


+1VALWP	
TDC -->	5.12A
Peak -->	7.212 A
OCF -->	8 A

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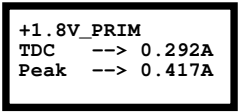
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```
+1.5V_RUN
TDC    --> 0.47A
Peak   --> 0.671A
```



```
+1.8V_PRIM
TDC    --> 0.292A
Peak   --> 0.417A
```

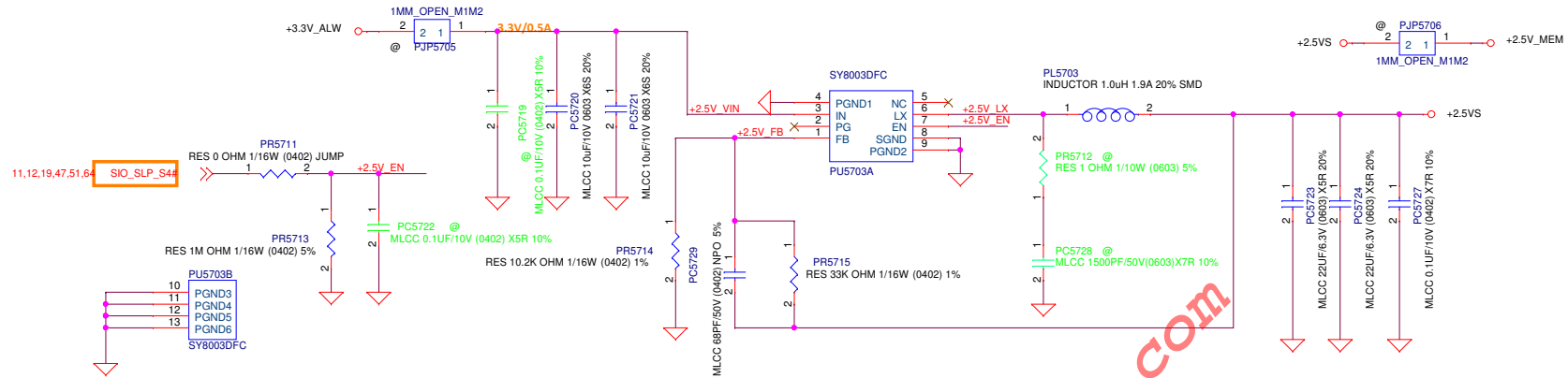


TITLE +1.5V_RUN/+1.8V_PRIM		
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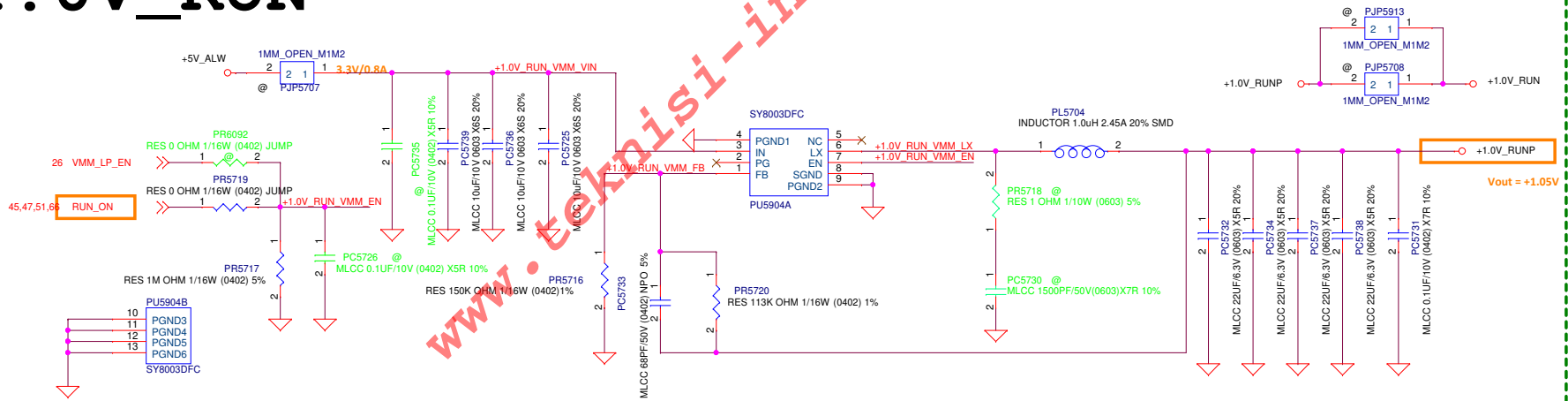
+2.5V_MEM

+2.5V_MEM
TDC --> 0.45A
Peak --> 0.6A



+1.0V_RUN

+1.0V_RUN_VMM
TDC --> 1A
Peak --> 2.1A



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TITLE	+2.5V_MEM/+1.0V_RUN_VMM	
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Place PH5805 Near PL5906

Place PH5801 Near PU5903

Place PH5804 Near PU5901

Place PH5802 Near PL5905

Place PH5602 Near PL5901

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TITLE: +VCC_CORE Controller DWG NO.: CORE_B2 DATE: Friday, March 18, 2016	REV: 2.0 SHEET 09 of 01




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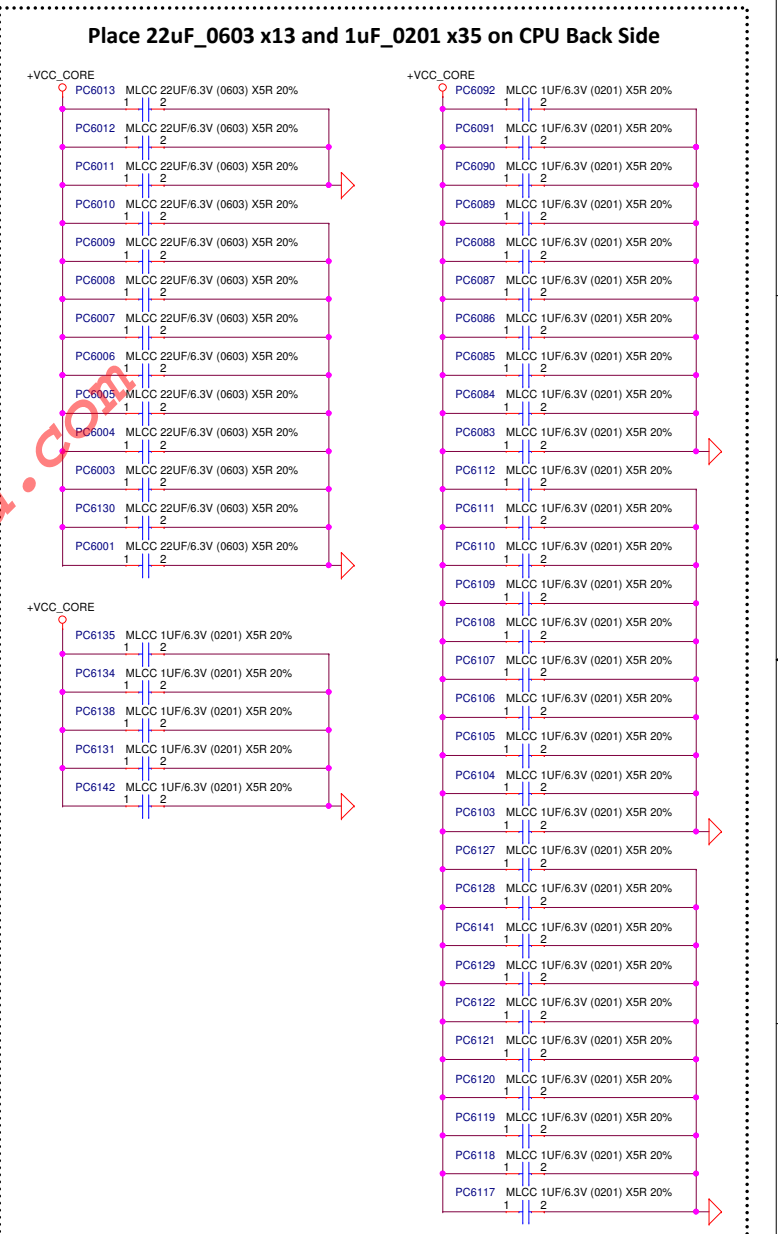
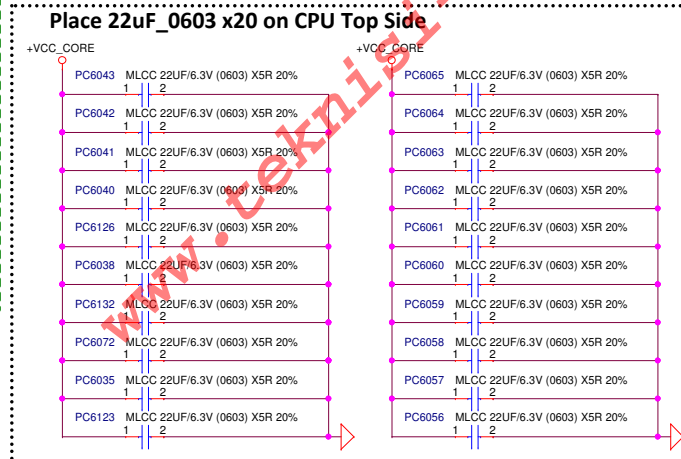
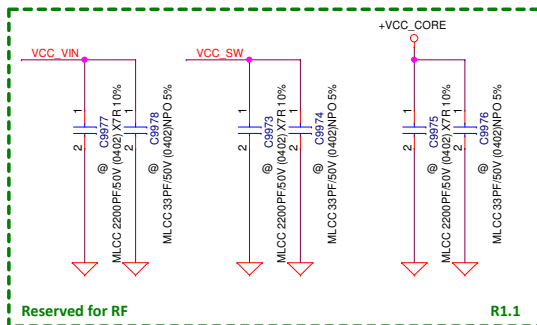
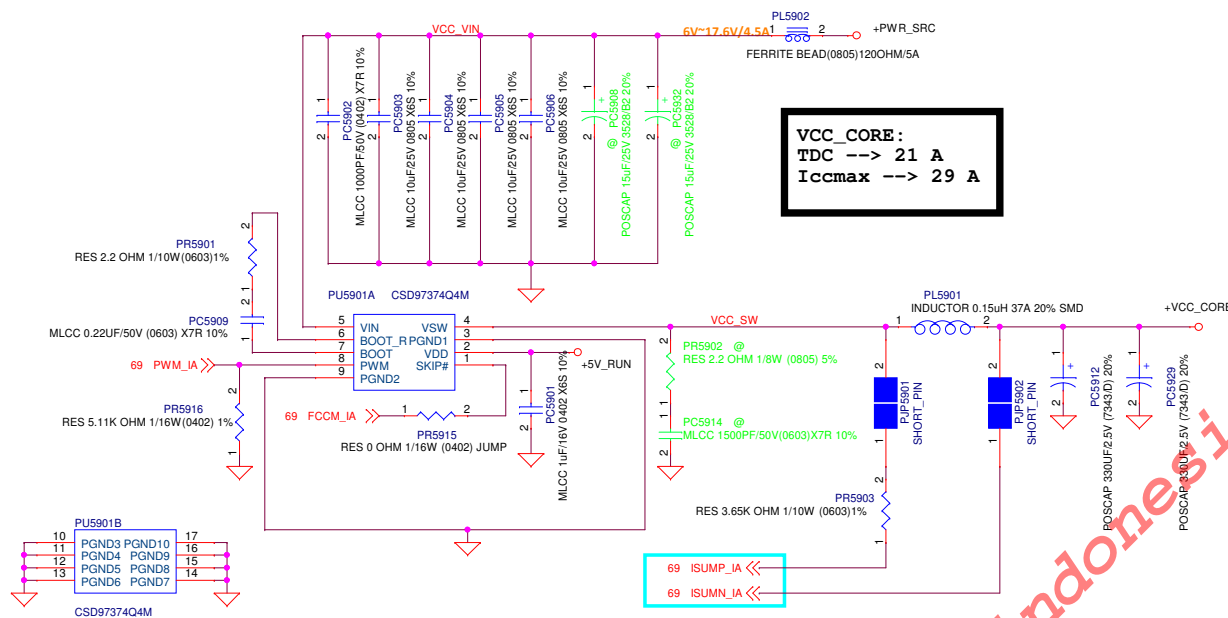
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+VCC_CORE Gate Driver



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TITLE	+VCC_CORE Gate Driver
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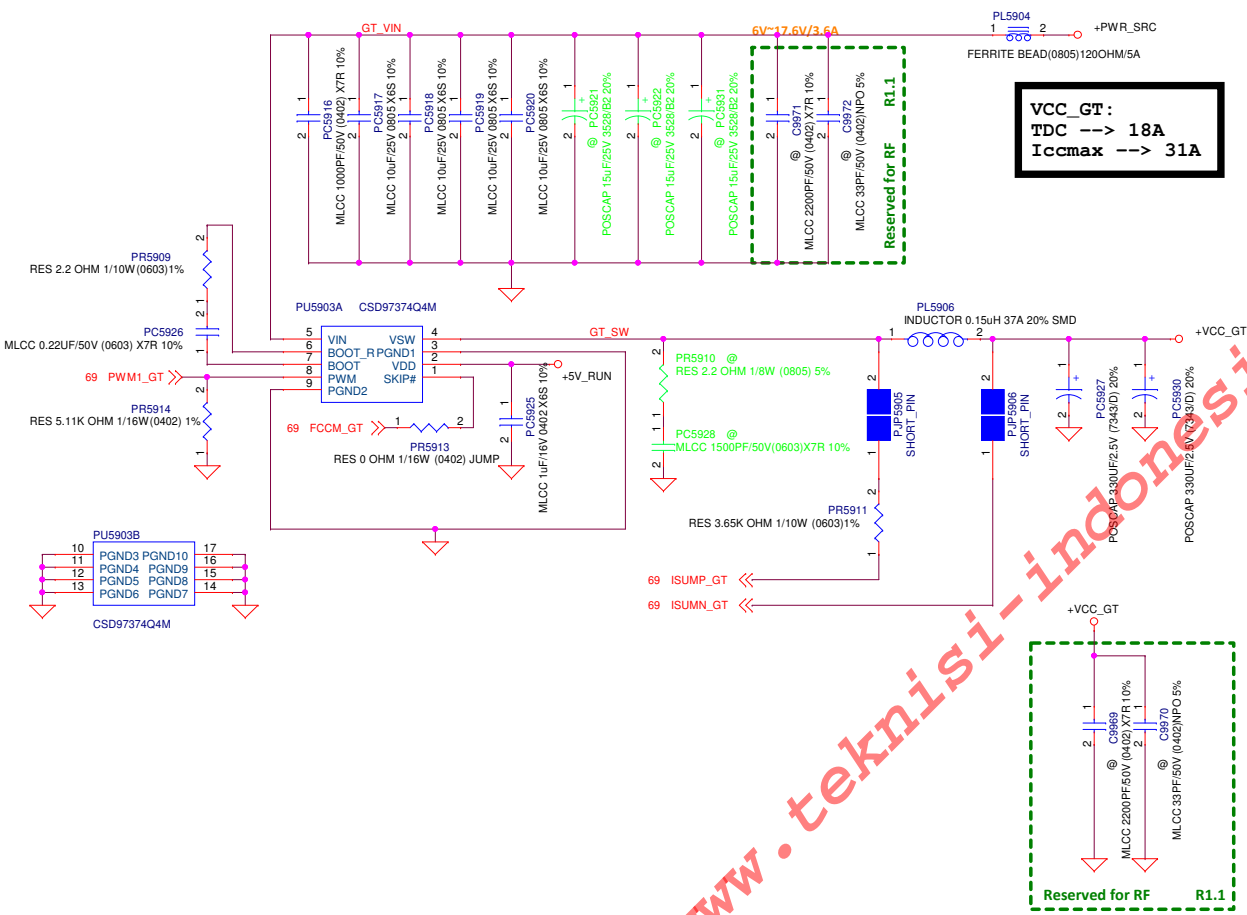
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CORE B2

REV. 2.0



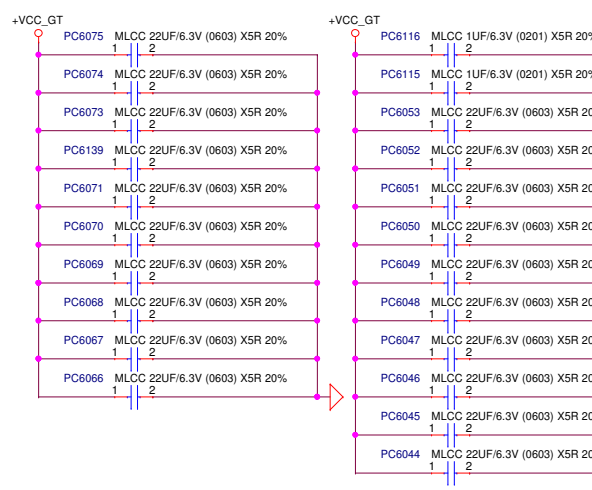
+VCC_GT Gate Driver



Place 22uF_0603 x13 and 1uF_0201 x12 on CPU Back Side



Place 22uF_0603 x20 and 1uF_0201 x2 on CPU Top Side

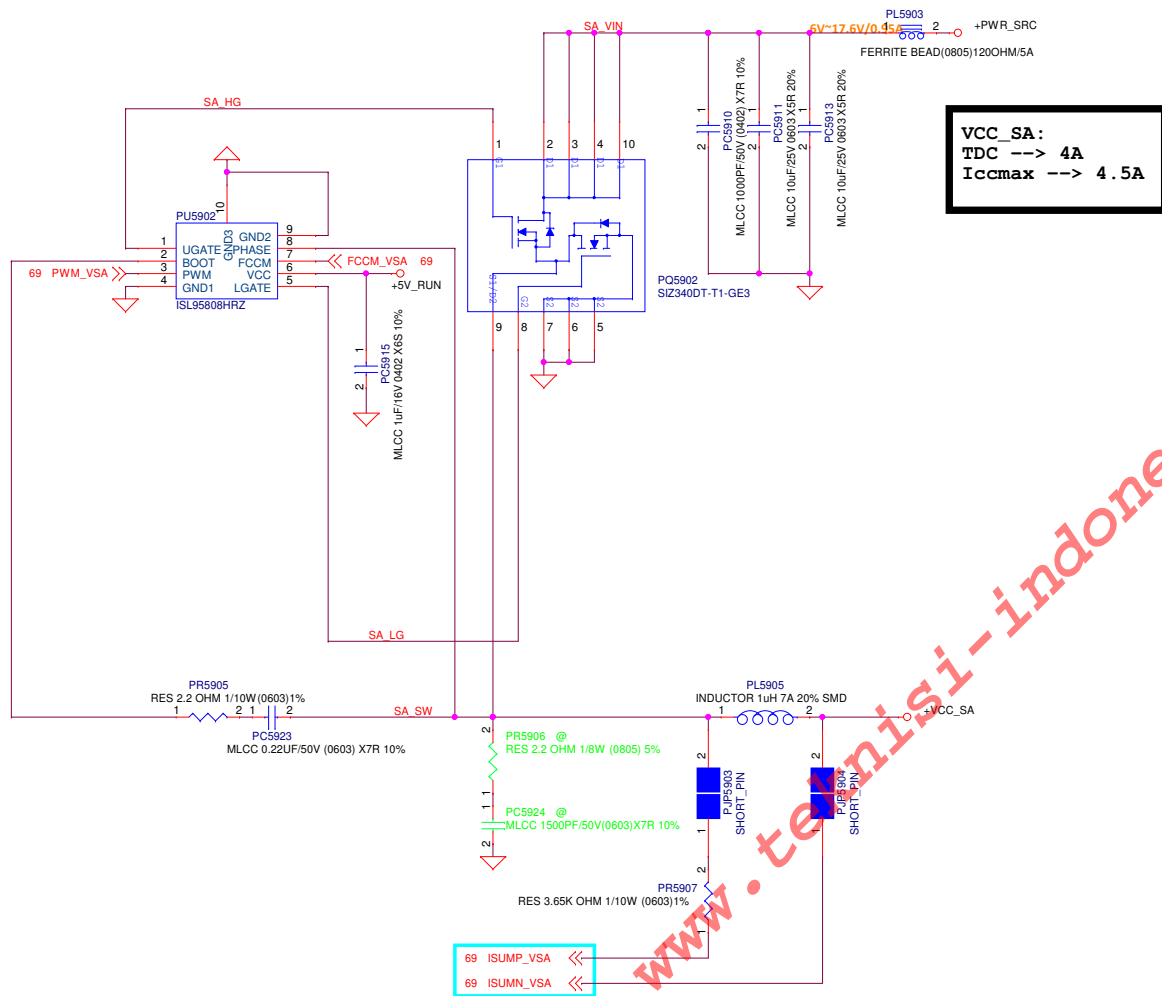


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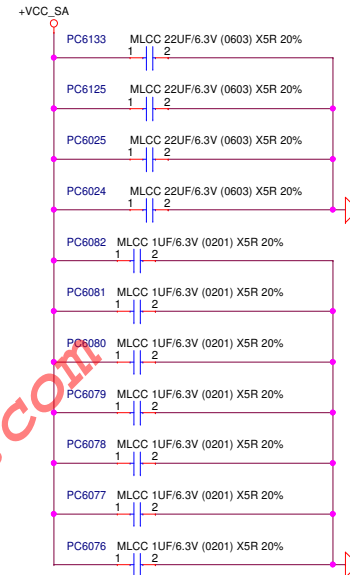
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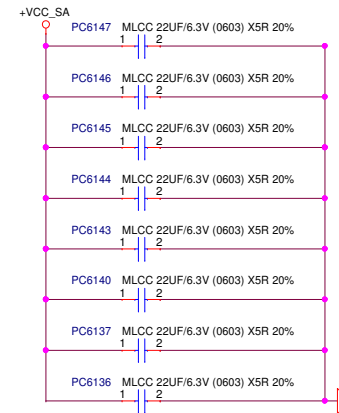
+VCC_SA Gate Driver



Place 22uF_0603 x4 + 1uF_0201 x7 on CPU Back Side



Place 22uF_0603 x8 on CPU Top Side



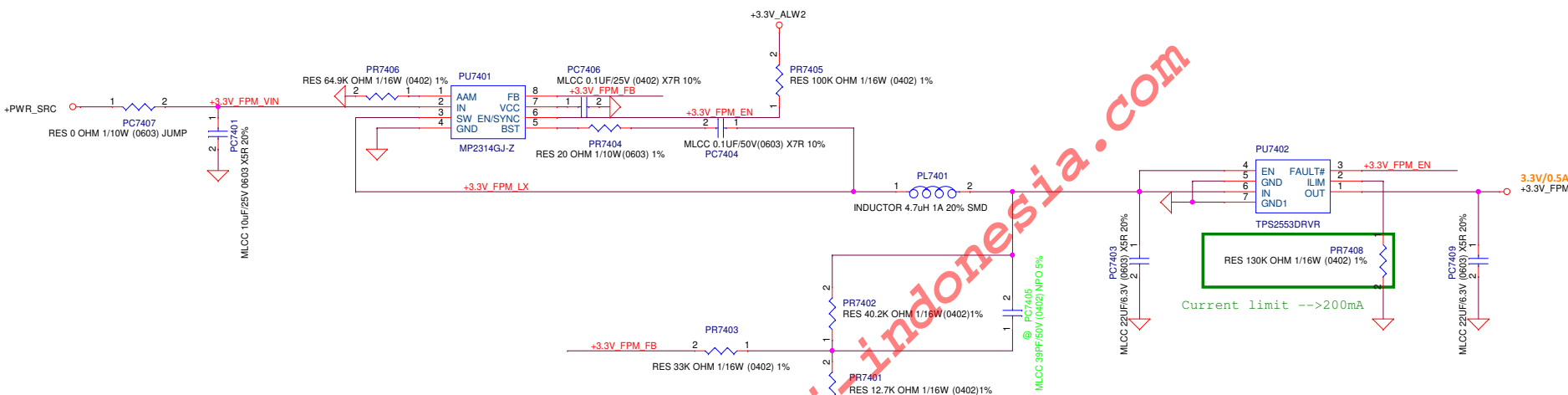
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+3.3V_FPM
Peak --> 0.5A



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TITLE +3.3V_FPM	
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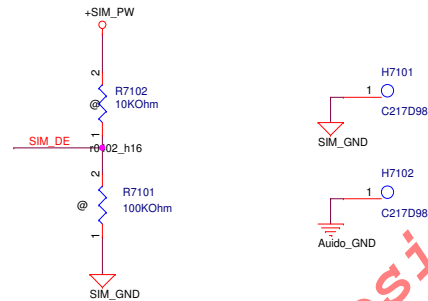
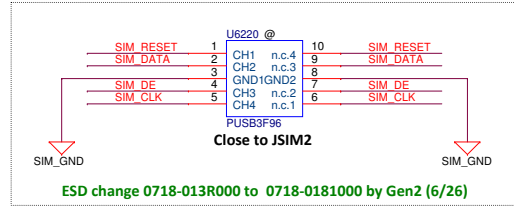
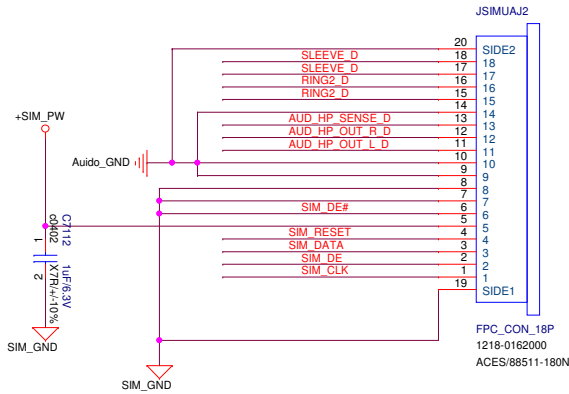
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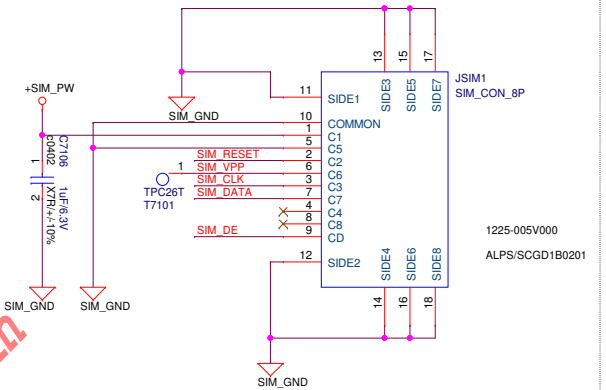
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ZIF Connector to MLB

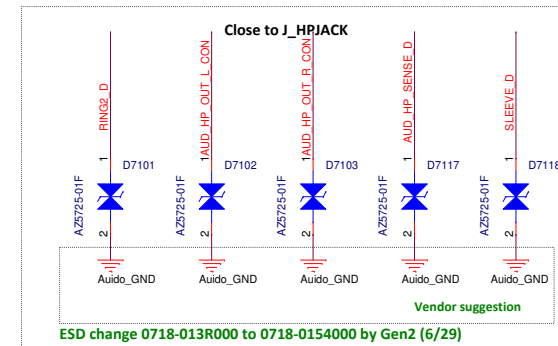
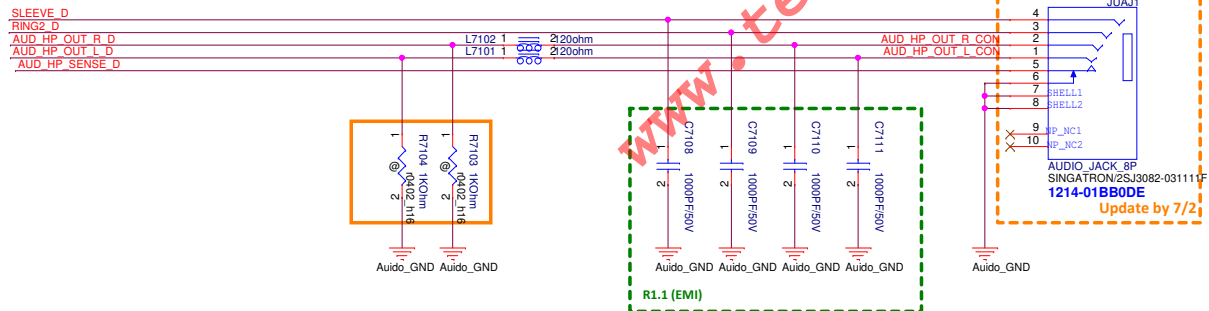


uSIM Card Push-Push



Audio Jack Connector

AUDIO COMBO PHONE JACK
auto sense OMTP and CTIA headset / support MIC-IN / HP & mono mic
SLEEVE_D & RING2_D LAYOUT TRACE WIDTH 80 mils

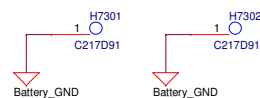
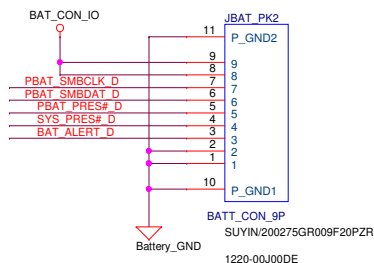


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The top diagram shows a component with pins 1 and 10 connected to P_GND1, which is then connected to Battery_GND. The bottom diagram shows a component with pins 1 and 10 connected to H7301 and C217D91, which are then connected to Battery_GND.

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